Hammad M. Cheema
Reza Mahmoudi
Arthur H.M. van Roermund

60-GHz CMOS Phase-Locked Loops

Springer

60-GHz CMOS Phase-Locked Loops

Hammad M. Cheema • Reza Mahmoudi •
Arthur H. M. van Roermund

60-GHz CMOS Phase-Locked Loops

Springer

Hammad M. Cheema
Eindhoven University of
Technology
Electrical Engineering
Den Dolech 2
5600 MB Eindhoven
Netherlands
h.m.cheema@tue.nl

Reza Mahmoudi
Eindhoven University of
Technology
Electrical Engineering
Den Dolech 2
5600 MB Eindhoven
Netherlands
r.mahmoudi@tue.nl

Dr. Arthur H. M. van Roermund
Eindhoven University of
Technology
Dept. Electrical Engineering
Eindhoven
Netherlands
a.h.m.v.roermund@tue.nl

ISBN 978-90-481-9279-3 e-ISBN 978-90-481-9280-9
DOI 10.1007/978-90-481-9280-9
Springer Dordrecht Heidelberg London New York

Library of Congress Control Number: 2010930220

Cover design: eStudio Calamar S.L.

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

Contents

Acronyms

AMOS	Accumulation metal oxide semiconductor
CMOS	Complementary metal oxide semiconductor
CP	Charge pump
DCM	Distributed capacitance model
DM-FD	Dual modulus frequency divider
DSP	Digital signal processing
DUT	Device under test
DVCO	Distributed voltage controlled oscillator
EMF	Electromotive force
FCC	Federal Communication Commission
FF	Flip-flop
FOM	Figure of merit
FSR	Frequency of self resonance
FTR	Frequency tuning range
GaAs	Galium arsenide
HBT	Heterojunction bipolar transistor
HDMI	High definition multimedia interface
HDTV	High definition television
IC	Integrated circuit
IF	Intermediate frequency
ILFD	Injection locked frequency divider
ISF	Impulse sensitivity function
ISS	Impedance standard substrates
LPF	Low pass filter
LO	Local oscillator
MC	Modulus control
MCML	MOS current mode logic
MIM	Metal–insulator–metal
PFD	Phase frequency detector
PDA	Personal digital assistant

PLL	Phase-locked loop
PM	Phase margin
PMP	Portable media player
PN	Phase noise
Q	Quality factor
RF	Radio frequency
RFD	Regenerative frequency divider
RFIC	Radio frequency integrated circuits
SA	Spectrum analyzer
SCL	Source coupled logic
SFD	Static frequency divider
SG	Signal generator
SiGe	Silicon germanium
SoA	Silicon on anything
SOI	Silicon on insulator
TSPC	True single phase clocking
TWD	Travelling wave divider
UWB	Ultra wide-band
VCO	Voltage controlled oscillator
VNA	Vector network analyzer
WLAN	Wireless local area networks
WPAN	Wireless personal area networks

Chapter 1
Introduction

Abstract This chapter lays the foundation for the work presented in latter chapters. The potential of 60 GHz frequency bands for high data rate wireless transfer is discussed and promising applications are enlisted. Furthermore, the challenges related to 60 GHz IC design are presented and the chapter concludes with an outline of the book.

Keywords Wireless communication · 60 GHz · Millimeter wave integrated circuit design · Phase-locked loop · CMOS

Communication technology has revolutionized our way of living over the last century. Since Marconi's transatlantic wireless experiment in 1901, there has been tremendous growth in wireless communication evolving from spark-gap telegraphy to today's mobile phones equipped with Internet access and multimedia capabilities. The omnipresence of wireless communication can be observed in widespread use of cellular telephony, short-range communication through wireless local area networks and personal area networks, wireless sensors and many others.

The frequency spectrum from 1 to 6 GHz accommodates the vast majority of current wireless standards and applications. Coupled with the availability of low cost radio frequency (RF) components and mature integrated circuit (IC) technologies, rapid expansion and implementation of these systems is witnessed. The downside of this expansion is the resulting scarcity of available bandwidth and allowable transmit powers. In addition, stringent limitations on spectrum and energy emissions have been enforced by regulatory bodies to avoid interference between different wireless systems.

At the same time, driven by customer demands, the last 2 decades have also experienced unprecedented progress in wireless portable devices capable of supporting multi-standard applications. The allure of "being connected" at anytime anywhere and desire for untethered access to information and entertainment "on the go" has set the ever increasing demand for higher data rates. As shown in Fig. 1.1, contemporary systems are capable of supporting light or moderate levels of

H.M. Cheema et al., *60-GHz CMOS Phase-Locked Loops*,
DOI 10.1007/978-90-481-9280-9_1,

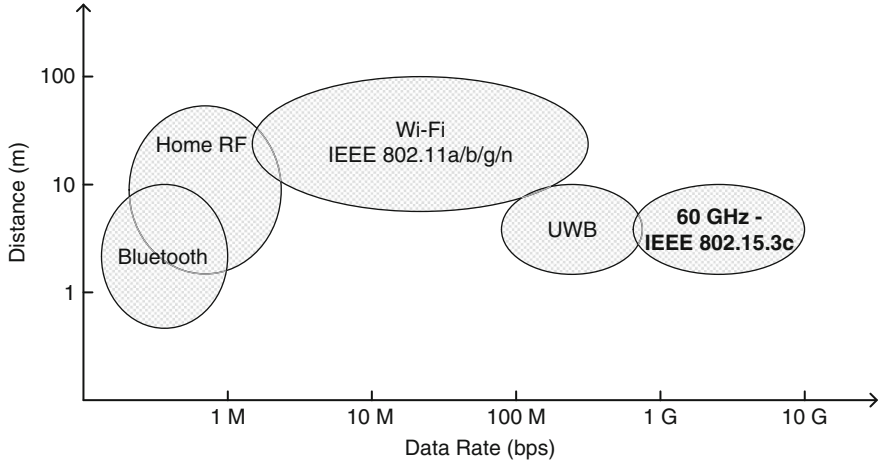

Fig. 1.1 Data rate and distance comparison for different WPAN and WLAN technologies

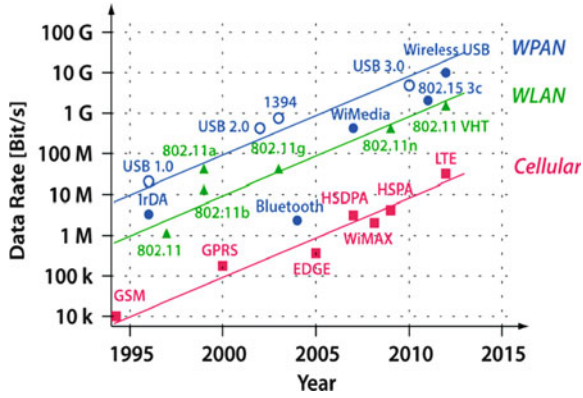

Fig. 1.2 Increasing data rate trend according to Edholm's law [2]

wireless data traffic, as in Bluetooth and wireless local area networks (WLANs). However, they are unable to deliver data rates comparable to wired standards like gigabit Ethernet and high-definition multimedia interface (HDMI) [1]. Furthermore, as predicted by Edholm's law [2], the required data rates (and associated bandwidths) have doubled every 18 months over the last decade. This trend is shown in Fig. 1.2 for cellular, wireless local area networks and wireless personal area networks for last 15 years.

The current standards and applications operating between 1 and 6 GHz have their market for long distance communication; however, in order to address the spectrum congestion and data rate issues mentioned above, new solutions have to be explored. As stated by Shannon [3], the maximum available capacity of a communication system increases linearly with channel bandwidth and

logarithmically with the signal-to-noise ratio. Therefore, the obvious choice is to look upwards in the frequency spectrum where more bandwidth could be available.

An intermediate solution offered was the introduction of ultra-wide band (UWB) in 2002 by the Federal Communications Commission (FCC). It offers the frequency spectrum from 3.1 to 10.6 GHz and a minimum required bandwidth of 500 MHz for its applications. Although UWB partially solves the bandwidth issue and can potentially support high data rates, there are some limitations hindering its popularity. Firstly, international coordination is difficult to achieve among major countries and IEEE standards are not accepted worldwide. Secondly, as UWB is an overlay system over the existing 2.4 and 5 GHz unlicensed bands used for already deployed WLANs, the inter-system interference is a major concern. In order to safeguard the existing wireless systems in different regions, local regulatory bodies have defined their own requirements for UWB making world-wide harmonization of UWB almost impossible. Furthermore, to avoid interference, the allowed transmit power is low giving rise to reliability concerns. Thirdly, current multi-band orthogonal frequency division multiplexing (MB-OFDM) based UWB systems can provide data rates uptil 480 Mbps which can only support compressed video. Uncompressed high-definition television (HDTV) can easily require 2 Gbps or more data rate, which although possible by enhancing MB-OFDM UWB, increases the complexity, cost and power consumption many folds. Lastly, variation of the received signal strength over the entire UWB spectrum poses sensitivity problems for the receiver [4, 5].

The above constraints of interference, transmit power and low data rate motivated the exploration of completely unoccupied frequency band in the millimeter wave (mm-wave) regime and 60 GHz appeared as one of the promising candidates for the purpose.

In 2001, spurred by the increasing demand of high data rate applications and limitations of current wireless technologies, a 7 GHz contiguous bandwidth was allocated world-wide by the FCC. There was an immediate interest, both in academia and industry, to investigate the opportunities and possibilities using this large chunk of bandwidth. The fact that this band was unlicensed further helped in triggering the research effort. The regional regulatory bodies allocated local frequency bands with slight shift and defined the maximum effective isotropic radiated power (EIRP). Table 1.1 lists these two parameters for different regions.

The maximum allowed EIRP at 60 GHz is much higher than other existing WLANs and WPANs. This is essential to overcome the higher space path loss (according to classic Friis formula) and oxygen absorption of 10–15 dB/km as shown in Fig. 1.3 [6]. These two loss mechanisms dictate the use of 60 GHz for short range multi-gigabit per second transmission. The attenuation also means that

Table 1.1 Regional spectrum allocation and emission power requirements

Region	Frequency band (GHz)	Max. EIRP (dBm)
Europe	59–66	57
Canada/USA	57–64	43
Korea	57–64	43
Japan	59–66	57
Australia	59.4–62.9	51.8

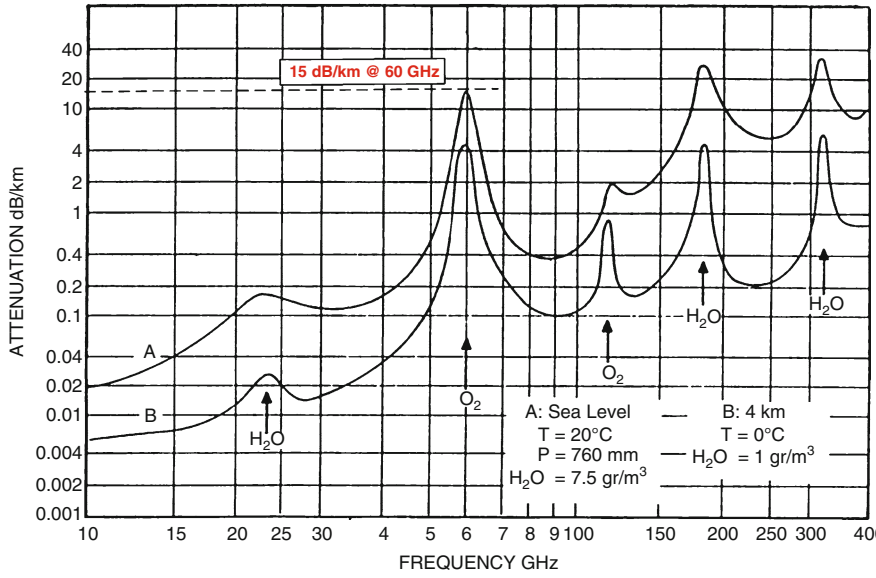

Fig. 1.3 Gaseous absorption at 60 GHz [6]

the system provides inherent security, as radiation from one particular 60 GHz radio link is quickly reduced to a level that does not interfere with other 60 GHz links operating in the same vicinity. Furthermore, this reduction enables the ability for more 60 GHz radio-enabled devices to successfully operate within one location.

Using the 60 GHz band for high data rate and indoor wireless transmission, a multitude of potential applications can be envisioned. The high definition multimedia interface (HDMI) cable could be replaced by a wireless system, transmitting uncompressed video streams from DVD players, set-top boxes, PC's to a TV or monitor. Current wireless HDMI products utilize the 2.5 and 5 GHz unlicensed spectrum where bandwidth is limited. As a result, these systems implement either lossy or lossless compression, significantly adding component and design cost, digital processing complexity and product size. Typical distance between these gadgets is 5–10 m and this communication can be point-to-point or point-to-multipoint. Depending on the resolution and pixels per line, the data rate required can vary from several hundred megabit per second (Mbps) to a few gigabit per second (Gbps). For instance, a typical high definition television (HDTV) offers a resolution of 1,920 × 1,080 with a refresh rate of 60 Hz. Assum-ing RGB video format with 8 b per channel per pixel, the required data rate is approximately 3 Gbps [1]. The future HDTV generation is expected to offer higher refresh rates as well as higher number of bits per channel scaling the required data rate beyond 5 Gbps. Therefore, transmitting HDTV transmission using 60 GHz remains an attractive test-case in the research field. Similarly, video and audio streams from personal digital assistant (PDA), portable media player (PMP) and laptops can also be transferred wirelessly to a display device.

In an office or home environment, 60 GHz radio links can essentially replace the clutter of cables of standards like USB, IEEE 1394, gigabit Ethernet and multimedia delivery. A PC can "talk" to all the external peripherals including printers, DVD writers, camcorders, digital cameras, external hard-disks and so forth. Wireless gigabit Ethernet and wireless ad hoc networks using 60 GHz are attractive applications for a conference room or library environment. A commercial application, particularly interesting for youth, is the so-called "Kiosk file downloading" in which users can download movies, games etc from a kiosk placed at locations like airports, railway-stations, market places and so on. These application examples are summarized in Fig. 1.4.

In addition to home and office, 60 GHz vehicular applications are also gaining much attention. They can be partitioned in three classes namely [4, 5]:

- Intra-vehicle wireless networks can be considered as a subset of WPANs that exist completely within a vehicle. The possibility of broadband communication within an automobile or aircraft by removing wired connections is desirable for manufacturers. The 60 GHz band is especially suited for intra-vehicle applications due to the containment within the vehicle and reduced ability to interfere with other vehicular networks.
- Inter-vehicle wireless networks are different from the intra-vehicle networks due to the outdoor propagation environment in the former. Applications like delivery of traffic information and range extension of mobile broadband networks are possible using inter-vehicle networks at 60 GHz.
- Vehicular radar, the last class of vehicular applications, has been deployed at millimeter-wave frequencies other than 60 GHz before; however, adaptive cruise control and automotive localization using the 60 GHz band have attracted interest in recent times.

Despite many advantages and attractive applications of short range gigabit per second wireless transmission at 60 GHz, a number of technical challenges related to design and performance need to be addressed. These can be broadly categorized into channel propagation issues, antenna technology, modulation schemes and integrated circuit technology and design.

In the last category, the choice of IC technology depends on the implementation aspects and system requirements. The former is related to the issues such as power consumption, efficiency, linearity and so on, while the latter is related to the transmission rate, cost and size, modulation etc. There are three competing IC technologies at mm-wave namely:

- Group III-V, such as Gallium Arsenide (GaAs) and Indium Phospide (InP). This technology offers fast, high gain and low noise circuits but suffers from poor integration and expensive implementation.
- Silicon germanium (SiGe) technology, such as heterojunction bipolar transistor (HBT) and BiCMOS are cheaper alternatives of GaAs and offer comparable performance.

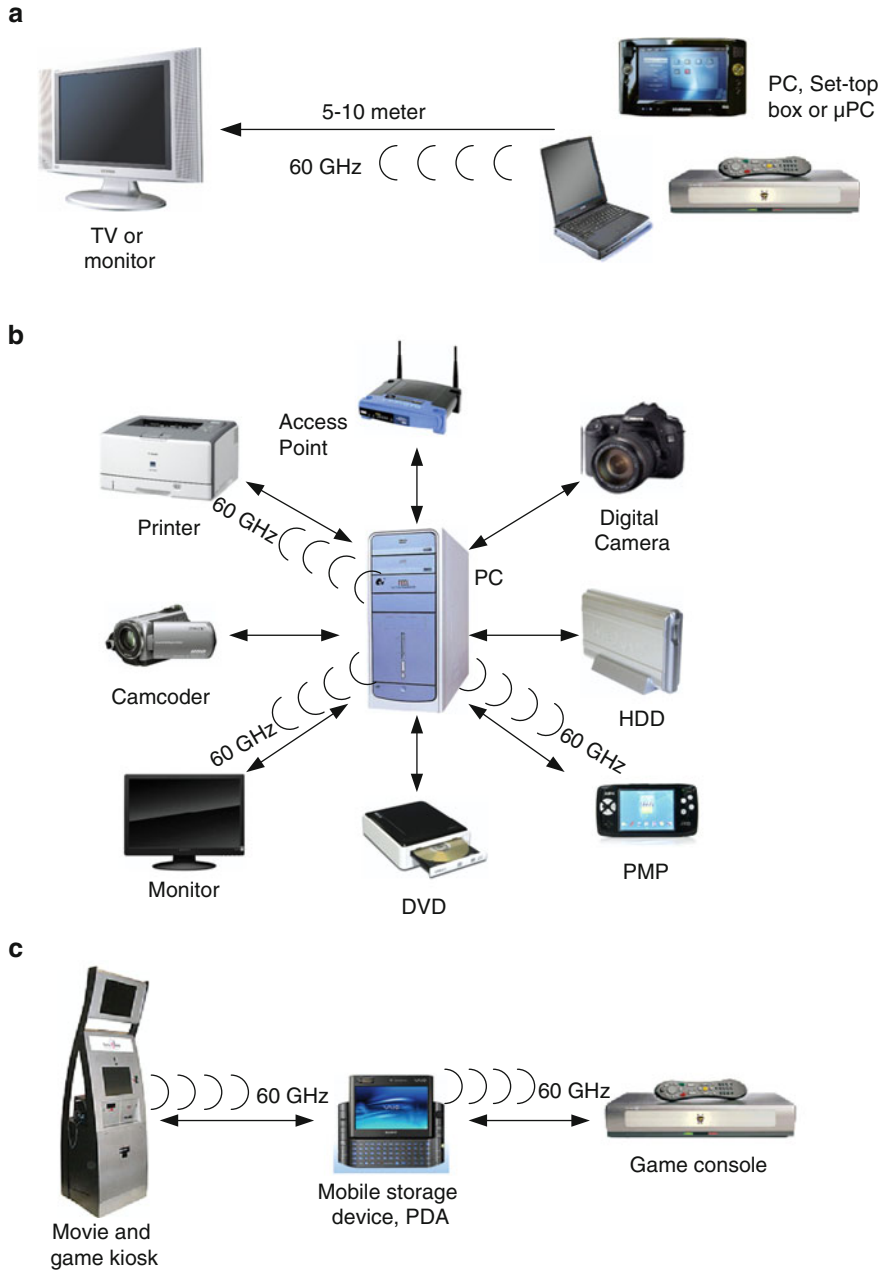

Fig. 1.4 Potential 60 GHz applications: point-to-point HDTV transmission (**a**), communication between a PC and different peripherals (**b**) and kiosk file downloading (**c**)

- Silicon technology, such as CMOS and BiCMOS. As size and cost are key factors for mass market production and deployment, CMOS technology appears to be the leading candidate as it offers high level of integration and is economical as compared to other alternatives. The downside of using CMOS is performance degradation due to low gain, linearity constraints, poor noise, low transition frequency (f_T) etc. However, the recent advances in CMOS technology, like silicon-on-insulator (SOI) and silicon-on-anything (SOA), coupled with continuous down-scaling to sub-nanometer technologies is facilitating the implementation of integrated circuits at 60 GHz. Furthermore, high speed digital signal processing (DSP) capabilities required for processing gigabit per second data is also possible using CMOS.

In order to circumvent the abovementioned performance limitations of CMOS, especially for phase-locked loops (PLLs), number of transceiver architectures have been proposed [7–18]. These methods generally aim to reduce the working frequency of the PLLs so that up-conversion or down-conversion of the signals is carried out at a lower frequency or in two steps. Furthermore, depending on the envisioned applications, one architecture might be preferred over another.

At circuit level design, the challenges are multi-fold. Low frequency circuits are not easily scalable to 60 GHz as the foundry transistor models are usually not characterized uptil this frequency. The parasitic elements of transistors also contribute to reduced high frequency performance. Consequently, considerable design margins have to be maintained resulting in power and silicon area penalty. Furthermore, few initial dry-runs are required to characterize the devices resulting in increased design times. Similarly, passives such as inductors and transformers etc., though become affordable in terms of silicon footprint, pose modeling related uncertainties and require meticulous electromagnetic (EM)-simulations. The quality factor (Q-factor) of varactors, which are invariably employed for capacitive tuning in voltage controlled oscillators (VCOs), frequency dividers etc, becomes very low. Low-ohmic substrate is also a hindrance in high-Q passive design. The technology scaling to sub-nanometer technologies reduces the supply and breakdown voltages, whereas the threshold voltage of transistors does not scale with the same order, resulting in a limited choice of reliable circuit topologies.

At layout level, as the wavelength of on-chip signals approach circuit dimensions, the interconnect between components becomes crucial part of design. These interconnects have to be simulated in EM solvers to incorporate the affect on circuit performance. Depending on the type of interconnect, this step is generally time consuming especially if multiple metal layers and vias are included. Furthermore, due to close proximity of components the overall layout also needs to be simulated for unwanted coupling and losses. Layout parasitics are also a major contributor for frequency shift and performance degradation and demand careful RLC extraction. Asymmetric layout of the RF paths at 60 GHz is a potential issue especially in circuits requiring phase accuracy. The typical layout approach of “smaller the better” at 60 GHz is sometimes contradictory to the symmetry requirement and some compromise has to be adopted.

The measurement of 60 GHz and millimeter wave circuits, pose a different set of challenges. Dedicated measurement equipment, components and setup is required for high frequency measurements. In some cases, when direct measurement of a parameter is not possible, in-direct methods are employed which are source of measurement errors. In order to shift the measurement plane to the device-under-test (DUT), accurate calibration and de-embedding is required. The losses and mismatch associated with cables, connectors, adapters have to be carefully accounted for. The stability and repeatability of accurate measurements is also an important challenge in high frequency measurements.

The challenges at 60 GHz related to circuit, layout, measurement and technology, mentioned in the preceding discussion, assist to select the set of problems which will be tackled in this book.

Firstly, due to the application dependence, there is no preferred transceiver architecture for 60 GHz. Thus, several different architectures can be expected in future. In order to cater for more than one application, a flexible synthesizer architecture will therefore be required. Moreover, such a multipurpose synthesizer will be expected to reuse some of its components to reduce design overhead. Secondly, a lack of design paradigm for 60 GHz is witnessed where the layout intricacies and measurement issues are understudied and lastly, the profound impact of parasitics necessitates the need of modification in the design flow of mm-wave integrated circuits. Adopting a top-down approach, this book addresses the above three problems by:

- System level analysis, design and realization of a flexible phase-locked loop suitable for a number of frequency up/down-conversion choices in a 60 GHz transceiver.
- Identifying the critical components of the synthesizer and characterizing them individually before complete system integration.
- Characterizing of passives, such as inductors, transformers and transmission lines that are extensively utilized in 60 GHz IC design.
- Revisiting the mm-wave IC design flow and incorporating the impact of parasitics (from circuit as well as layout) at an advanced stage of the design cycle.
- Identifying measurement issues for mm-wave circuits and providing possible solutions.

The structure of this book is illustrated in Fig. 1.5. In Chapter 2, after a brief overview of IEEE standardization for 60 GHz band and frequency conversion choices, a flexible PLL architecture is proposed. Based on theoretical analyses and system simulations of this architecture, target specifications are laid down for the PLL.

Chapter 3 discusses the layout and measurement techniques widely employed throughout this work. The circuit design of PLL components is divided in two chapters. The high frequency components, namely prescaler and voltage control oscillator (VCO) are discussed in Chapter 4. A variety of prescaler architectures are compared and two types are designed and measured. A number of VCOs are designed and measured with attention on improvement of tank quality factor,

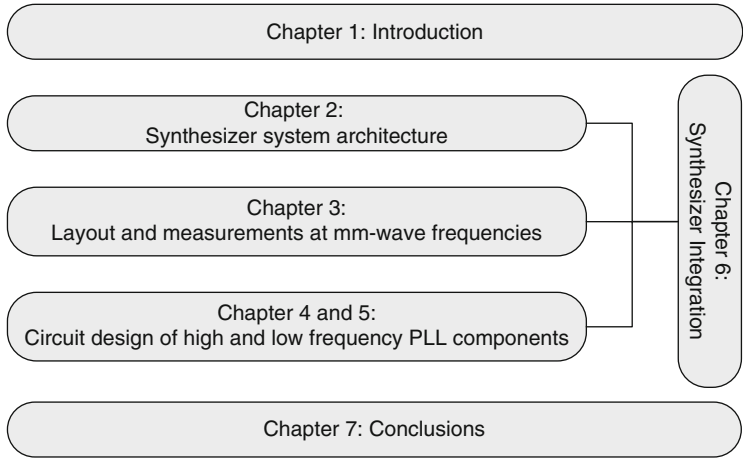

Fig. 1.5 Structure of the book

modeling of tank inductor and transformers, and compact and symmetrical layouting techniques. The low frequency components such as the feedback divider chain, phase frequency detector (PFD), charge pump (CP) and loop filter are presented in Chapter 5. Optimization techniques for feedback divider chain, dead-zone removal in PFD and accurate current matching in CP are also discussed in this chapter.

Chapter 6 presents the integration of the complete PLL and discusses solutions for different frequency conversion choices. It is observed that connecting different blocks with perfect frequency alignment is much more challenging than designing individual blocks. This is because any unexpected parasitic of the interface between the blocks can potentially cause significant shift in the VCO and dividers, causing reduction in PLL locking range or in worst case prohibiting the loop from locking. A comparison to target specifications is also included in this chapter. The conclusions of this book are presented in Chapter 7.

Chapter 2
Synthesizer System Architecture

Abstract This chapter discusses the system level aspects of frequency synthesizer design for 60 GHz. The IEEE 802.15.3c standard determines the frequency channelization of the 60 GHz band, based on which the frequency planning is carried out. A number of in-direct PLL architectures can be used for 60 GHz transceivers which are discussed in detail. Based on the proposed synthesizer architecture, the analytical calculations and system level simulations are presented. The chapter concludes by enlisting the target specifications for the proposed synthesizer.

Keywords IEEE 802.15.3c · 60 GHz · Phase-locked loop · Frequency synthesizer · Advanced design systems · Phase noise · Open-loop gain · Phase margin

A phase-locked loop is an important block of transceivers and exists in the majority of wireless communication systems. Its application varies from generation, recovery and distribution of clock signals to jitter and noise reduction. They are also utilized to implement spread spectrum techniques to reduce interference with high-Q receivers and as a de-skewing block to phase match the clock in electronic systems. The most extensive use of PLLs is for frequency synthesis (also focus of this book), in which they are used to generate a local oscillator signal for up-conversion in a transmitter and down-conversion in a receiver as shown in Fig. 2.1. The requirements and architecture of a synthesizer depend on the system specifications which are based on the underlying regulatory standard. Performance parameters like tuning range, channel spacing or step size, spectral purity, phase noise, output power, settling time and spurious are some of the specifications required before the design phase.

The regulatory efforts for 60 GHz band are being carried at two fronts. IEEE has assigned a task group 3c for developing a millimeter-wave based alternative physical layer (PHY) for the existing 802.15.3 standard [19]. The second effort is by industrial consortiums such as WirelessHD™ and ECMA International. The WirelessHD alliance has proposed a protocol that enables consumer devices to create a wireless video area network for streaming high-definition content between source and display devices [20]. ECMA International on the other hand published its 60

H.M. Cheema et al., *60-GHz CMOS Phase-Locked Loops*,
DOI 10.1007/978-90-481-9280-9_2,

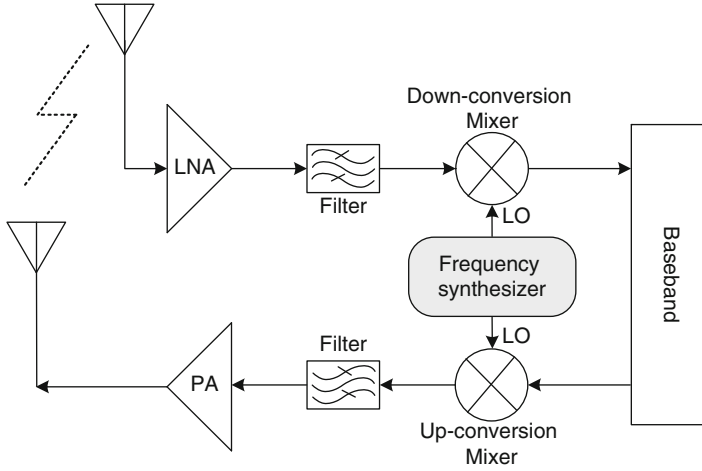

Fig. 2.1 A general transceiver block diagram

GHz industrial standard in December 2008. In addition to 60 GHz PHY, this standard includes MAC and HDMI PAL specifications for short range gigabit per second wireless transmission for both bulk data transfer and multimedia streaming [21]. Section 2.1 discusses the IEEE 802.15.3c channelization proposals with particular focus on PLL requirements.

Integrated circuits at 60 GHz involve significant challenges at system, circuit and layout levels as discussed in Chapter 1. However, some of these can be mitigated by taking advantage of the capabilities available at one level to relax the requirements imposed at another. For instance, to ease the requirements of a frequency synthesizer at system level, special transceiver architectures for up-conversion and down-conversion of data can be envisioned. Termed as frequency conversion (FC) techniques in this book they generally aim to operate the synthesizer at a sub-LO frequency and generate the 60 GHz LO signals indirectly. Adopting this approach makes a wide variety of architectures possible by selecting different LO frequency combinations along with the synthesizer. Consequently, each resulting architecture requires a specific synthesizer and a need for a flexible synthesizer is naturally felt. This chapter proposes a flexible PLL which can be utilized for a number of 60 GHz FC techniques. While minimizing overhead, the focus is to re-use a considerable portion of the PLL and provide flexibility at the same time. The 60 GHz FC techniques are categorized in Section 2.2, and Section 2.3 presents the proposed synthesizer architecture.

Analytical calculations and system simulations using tools such as Advanced Design System (ADS) provide a first insight into the required specifications of the PLL and its individual sub-components. Section 2.4 includes the theoretical analysis of the PLL system and, aided with simulations, leads to the target specifications mentioned in Section 2.6. The conclusions of the chapter are presented in Section 2.7.

2.1 IEEE 802.15.3c Channelization

The IEEE 802.15.3 Task Group 3c (TG3c) was formed in March 2005. It is developing a millimeter-wave-based alternative physical layer (PHY) for the existing 802.15.3 wireless personal area network (WPAN) standard 802.15.3-2003. The standard is still a work in progress, and when completed, is expected to provide the first widespread international physical layer framework to support consumer 60 GHz WPANs. In September 2007, after merging and narrowing down, the task group confined its selection for 60 GHz physical layer to two proposals. These two proposals offer different possibilities of spectrum occupancy, transmission modes, modulation schemes, packet and frame structure, beam forming etc.

The channelization proposals for the 60 GHz band are based on high rate PHY (HRP) and low rate (LRP). The use of each depends on the data rate requirement for a certain type of communication. The HRP, having a bandwidth of 2 GHz, is used for high definition video streaming, file transfer and similar applications where multi-gigabit per second data rate is required. The channelization is shown in Fig. 2.2. The LRP, on the other hand, is used for relatively low data rate asynchronous transfer such as compressed audio, control commands including pilot, beacon and acknowledgment signals, etc. There are two proposals for the low rate channelization which offer a bandwidth of 1 GHz or 500 MHz. The sub-channelization of four 2 GHz channels either contains four 1 GHz channels or twelve 500 MHz channels. The channelization for LRP is shown in Figs. 2.3 and 2.4, respectively.

It can be noted that the center frequencies for 1 and 2 GHz channels are identical and only differ in the guard band between two adjacent channels. The spectrum utilization of the 500 MHz sub-channels is better than the 1 GHz ones and at least

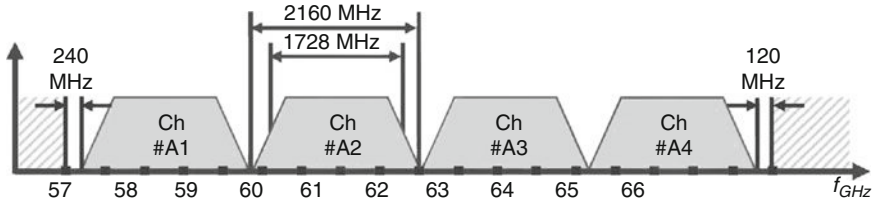

Fig. 2.2 High data rate channelization with 2 GHz bandwidth [19]

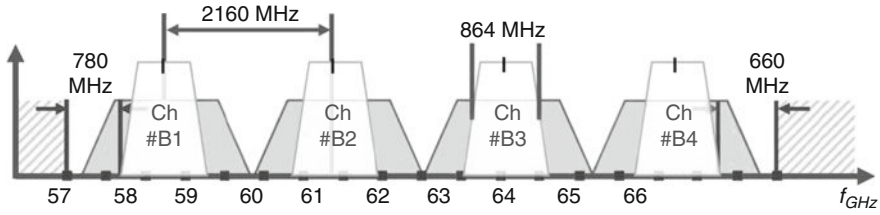

Fig. 2.3 Low data rate channelization with 1 GHz bandwidth [19]

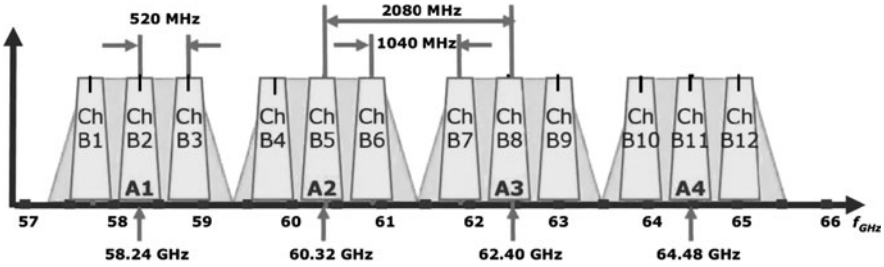

Fig. 2.4 Low data rate channelization with 500 MHz bandwidth [19]

nine out of 12 channels are available in all regions. The above mentioned channelization is important for a 60 GHz PLL design as it determines the frequencies required from the PLL and also some in-direct specifications such as reference frequency, loop bandwidth, etc. These proposals also indicate that, if such a channelization is finalized, the PLL should be able to generate all 2 GHz as well as all sub-channels of 1 GHz and 500 MHz.

2.2 60 GHz Frequency Conversion Techniques

As mentioned briefly in Chapter 1, the PLL (as frequency synthesizer) related challenges at millimeter wave frequencies is one of the dominating factors in transceiver design and necessitates the development of "synthesizer-friendly" transceivers. The generation, division and distribution of a mm-wave LO (signal used for up- and down-conversion) becomes so demanding that the choice of transmitter (TX) and receiver (RX) architectures become closely intertwined with the synthesizer design [22].

Therefore it is pertinent to categorize the approaches for up- and down-conversion (or frequency conversion) of data for 60 GHz transceivers which will also determine the associated synthesizer architectures. The general aim is to reduce the operation frequency of the synthesizer while maintaining a robust overall system.

The first category in Fig. 2.5a illustrates a two step down-conversion method, a special case of which is referred to sliding-IF architecture. The incoming RF signal f_{RF} is first down-converted by mixing with the RF local oscillator signal f_{RF-LO} producing a difference (and sum) component at $f_{RF} - f_{RF-LO}$. The second down-conversion to baseband is achieved by using the output of the prescaler of the frequency synthesizer f_{IF-LO}. The factor 'M' refers to an integer frequency multiplier which can have a usually range between 1 and 3. The value of 1 implies a direct connection between the oscillator and the mixer whereas a value of 2 and 3 implies a frequency doubler and tripler, respectively. The factor 'P' is the

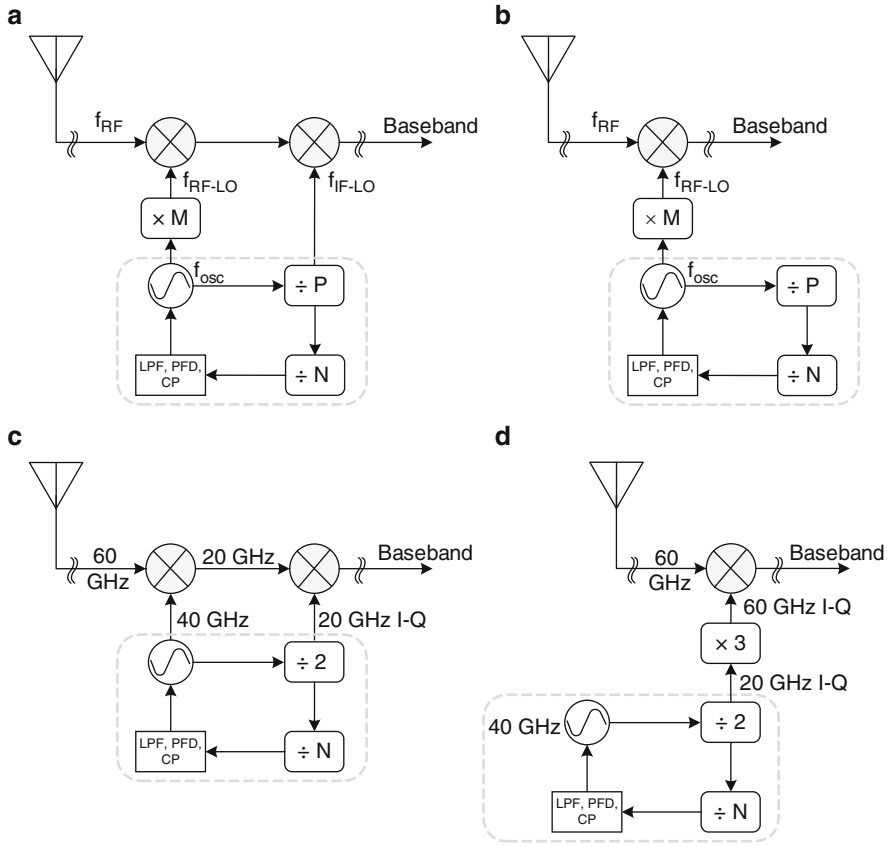

Fig. 2.5 Receiver architectures for different FC techniques: generalized two step down-conversion (sliding-IF) (**a**), generalized single step down-conversion (**b**), an example of two step down-conversion (**c**), and an example of single step down-conversion using a frequency tripler (**d**)

division ratio of the prescaler and can also have a value between 1 and 3. The overall division ratio of the synthesizer is separated into 'P' and 'N' as the prescaler requirements and utilization in millimeter-wave synthesizers is distinct from the lower frequency divider chain. The frequency conversion to baseband is carried out as

$$f_{RF} - (f_{RF-LO} - f_{IF-LO}) = 0 \tag{2.1}$$

where $f_{RF-LO} = f_{OSC} \times M$ and $f_{IF-LO} = f_{OSC} / P$. Therefore, (2.1) can be re-written as

$$\begin{aligned} f_{RF} - f_{osc} \times M &= \frac{f_{osc}}{P} \qquad \text{and} \\ f_{osc} &= f_{RF}\left(\frac{P}{MP+1}\right) \end{aligned} \tag{2.2}$$

Using values for M and P between 1 and 3 in (2.2) yields synthesizers operating at varying frequencies. For instance M = 1, P = 1 implies the synthesizer operates at 30 GHz and provides both the RF-LO and IF-LO signals. This architecture, termed as "half-RF", is presented in [13]. This solution, although offering the lowest possible LO without doublers or triplers, has two major drawbacks: third harmonic image and LO-IF feed-through.

The values M = 1, P = 2 yield a synthesizer operating at 40 GHz shown in Fig. 2.5c. The required quadrature IF-LO is provided by the prescaler to down-convert the 20 GHz IF signal to baseband. Another demonstrated architecture uses M = 3, P = 2 by operating the synthesizer at ~17 GHz and using a frequency tripler to down-convert the RF signal to 8.5 GHz. The conversion to baseband is again using the outputs of the prescaler [23]. Another interesting frequency conversion is achieved by using M = 2, P = 2 which uses 24 GHz synthesizer and 48 and 12 GHz as the first and second down-conversion steps. Other combinations for a two step down conversion are shown in Table 2.1.

The second category of frequency conversion techniques is based on a single step down-conversion using a f_{RF-LO} of 60 GHz as shown in Fig. 2.5b. In this case, the LO frequency can be obtained either directly from a synthesizer or indirectly by using a frequency multiplier (M) in combination with a synthesizer. For instance M = 1 yields a frequency synthesizer operating at 60 GHz. Termed as a direct conversion or zero-IF architecture, it uses 60 GHz quadrature LO from the synthesizer to down-convert the RF signal directly to baseband. In addition to the known issues of LO leakage, DC-offset and IP2, generation of accurate quadrature LO phases at 60 GHz, is a difficult task. In addition, division and distribution of 60 GHz LO also pose critical challenges [12, 22, 24]. For M = 3, Fig. 2.5d depicts a direct-conversion receiver with the synthesizer running at 40 GHz. The output in this case is obtained from the prescaler instead of the VCO as some prescaler architectures provide inherent quadrature signals and do not need extra circuits to generate I-Q outputs as in case of VCOs. The prescaler output is translated to a 60 GHz quadrature LO using a frequency tripler as presented in [25]. Another direct conversion topology is possible by using a 30 GHz synthesizer and a frequency doubler (M = 2) to generate 60 GHz quadrature LO signals. The use of frequency doublers and triplers, although reduces the synthesizer frequency, requires innovative design techniques to overcome their lossy behavior at these frequencies. Furthermore, generation and distribution of quadrature phases from these components has to be achieved.

Table 2.1 Synthesizer frequencies for different values of frequency multipliers (M) and prescaler division ratios (P)

M	P	f_{osc}(GHz)	f_{IF-LO}(GHz)
1	1	30	30
	2	40	20
	3	45	15
2	1	20	20
	2	24	12
	3	25.7	8.5
3	1	15	15
	2	17	8.5
	3	18	6

2.3 Proposed PLL Architecture: Flexible, Reusable, Multi-frequency

The considerable number of frequency conversion techniques elaborated in the previous section motivates the need for a flexible PLL system. The high frequency components of the synthesizer, namely VCO and prescaler are termed as the PLL front-end in this work, whereas the low frequency components including the divider-chain, phase frequency detector, charge pump and loop filter are labeled as the PLL back-end. The proposed synthesizer (shown in Fig. 2.6), while keeping the back-end fixed, aims to provide a flexible front-end enabling its application for a number of FC techniques.

The starting point of the proposed synthesizer is the architecture in Fig. 2.5c. The incoming RF signal is mixed with a nominal LO frequency of 40 GHz, generating an IF frequency of 20 GHz. The IF signal is then down-converted to baseband using the quadrature outputs from the first divider stage. This architecture, called sliding-IF, is different from its conventional dual-conversion counterpart as it requires only one synthesizer to generate the RF and IF local oscillator signals. The use of the sliding-IF topology offers the following advantages:

- The RF-LO generation takes place at 40 GHz without the need of quadrature phases.
- Using $f_{osc} = 2/3 \times F_{rf}$ reduces the required 60 GHz bandwidth (B) by the same factor, i.e. $2/3 \times B$ is needed at 40 GHz. This is especially beneficial as achieving 7 GHz of tuning range for VCOs at 60 GHz is a considerable challenge.
- The frequency division in the prescaler also occurs at 40 GHz increasing the possibility of utilizing different frequency divider topologies.
- Distribution and layout issues for 40 GHz differential LO are less severe than quadrature 60 GHz signals.

The second usage of the proposed PLL is shown in the direct-conversion topology of Fig. 2.5d where a frequency tripler, using the 20 GHz quadrature phases from the prescaler output, generates the 60 GHz quadrature LO signals. The requirement from an academic partner (in the WiComm project) for a 20 GHz quadrature LO further augments this choice and will be explained in the next section.

Another flexibility in the synthesizer topology is motivated by the possible re-usability of the PLL back-end. As shown in Fig. 2.6, by designing a dual-band or switchable VCO operating at 40- and 60 GHz, and a dual-mode (or switchable) prescaler capable of divide-by-2 and divide-by-3 operation, the proposed synthesizer can also operate in a direct-conversion topology without the frequency tripler. The re-usability of a power hungry and area consuming PLL back-end is a substantial advantage. However, meeting the performance specifications simultaneously, at 40- and 60 GHz, in these dual-mode components is a challenging part of design.

The divider chain, next to the prescaler usually consists of cascaded frequency dividers. In this work, we propose an alternative of the divider chain and replace it

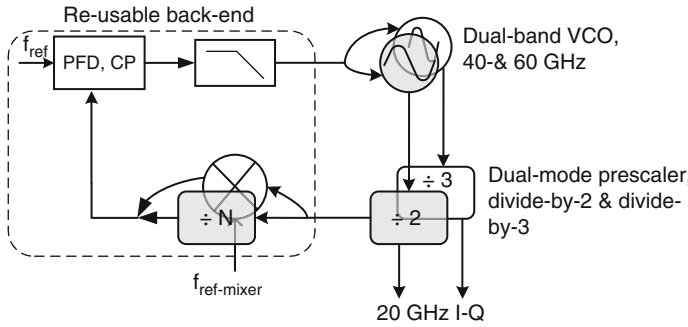

Fig. 2.6 Proposed PLL architecture suitable for sliding-IF and direct-conversion with and without tripler

with a mixer to directly down-convert the prescaler output frequency close to reference frequency for phase and frequency comparison. The different channelization proposals of the IEEE 802.15.3c standard explained in Section 2.1 signify the need for careful frequency planning of the synthesizer. The proposed synthesizer aims to support the 2 GHz HRP channels as well as 1 GHz and 500 MHz LRP channels, making it a multi-frequency PLL.

Summarizing, the proposed synthesizer envisions firstly, the sliding-IF topology, secondly, the direct-conversion topology with or without using a frequency tripler and, while using the same PLL back-end, to support all channelization proposals of the standard.

2.3.1 Utilization in WiComm Project

As mentioned in Chapter 1, the WiComm project aims to demonstrate an integrated 60 GHz transceiver. The transmitter part, being designed by an academic partner, is based on a frequency tripler, mixer and a power amplifier. The frequency tripler reported in [25] requires quadrature phases at 20 GHz to generate 60 GHz quadrature local oscillator signals. The key requirement from the synthesizer (of this work) is to provide 20 GHz quadrature signals with 0-dBm output power and a frequency range of 19–21 GHz, corresponding to an LO frequency of 57–63 GHz. On a system level, the proposed PLL topology is able to provide the required LO. The output power and frequency range specifications will be used during the circuit design of the synthesizer.

2.4 System Analysis and Design

Prior to actual circuit design, investigation of the complete PLL system analytically as well as by system simulations is required to gain insight into the overall requirements. This section, after discussing PLL basics and frequency planning, presents the

calculated system parameters such as phase margin, loop bandwidth and component specific parameters such as VCO gain, charge pump current and loop-filter values.

2.4.1 Phase-Lock Loop Basics

Phase-locked loops, as mentioned earlier, have a variety of applications. However, in this book we will focus on their use as a frequency synthesizer. In simple terms, using a clean reference signal (f_{ref}), a frequency synthesizer generates the channelized frequencies in order to up-convert the outgoing data for transmission and down-convert the received signal for processing.

A basic frequency synthesizer consists of a phase-frequency detector (PFD), charge-pump (CP), loop filter, VCO, high-speed prescaler as a first divide stage and a series of subsequent frequency dividers (see Fig. 2.7). Due to the feedback operation, the output frequency of the above synthesizer is given by

$$f_{out} = N \times P \times f_{ref} \tag{2.3}$$

Generally, the prescaler division factor (P) is included in the overall division factor. However, in mm-wave synthesizers the requirements for prescalers are much different than the lower frequency divider chain. Therefore, they will be

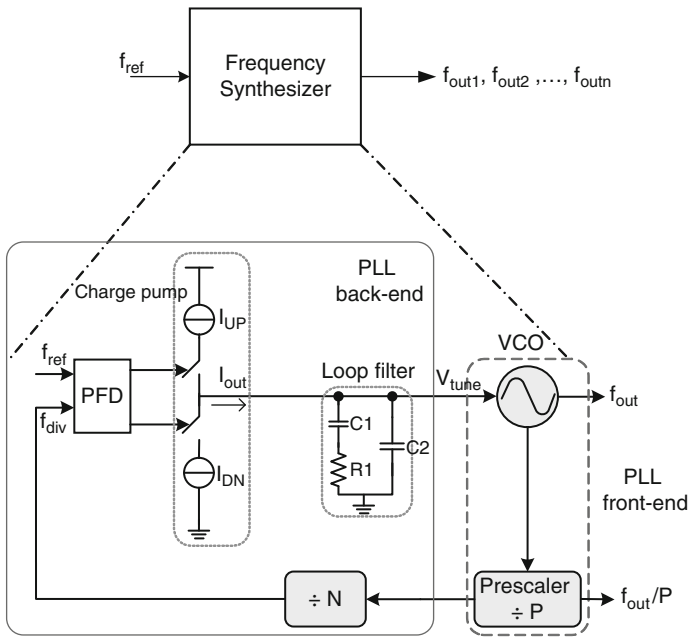

Fig. 2.7 Basic frequency synthesizer block diagram

treated separately in this work. Based on the type of frequency division, the synthesizer can be broadly categorized into the following:

- Integer-N frequency synthesizer, in which the division factor (N×P) is an integer. The frequency resolution or channelization, in this case, can only be equal to the reference frequency (f_{ref}). This can be a limitation for narrow-band applications where lower resolution is desired.
- Fractional-N frequency synthesizer, in which the division factor is a fractional number. Using such a synthesizer enables the use of a large reference frequency to achieve a small frequency resolution. The fractional division is achieved by employing dual-modulus or multi-modulus frequency dividers. The down-side of fractional-N synthesizers is the appearance of fractional spurs within the loop bandwidth which, for practical applications, have to be suppressed to an acceptable level. Techniques such as Sigma-Delta modulation have been used to control the loop divider such that fractional spurs can be randomized and shifted to a higher frequency band where they can be easily removed by the loop filter.

As this book targets the 60 GHz wireless transmission system which is a wide-band system, the main focus will be on integer-N frequency synthesizers.

The basic operation of a synthesizer starts with a clean reference signal (f_{ref}) which in most cases is a crystal oscillator. This acts as one input of the phase-frequency detector whereas the second input is the feedback signal from the divider chain (f_{div}). The PFD compares the incoming signals and generates voltage pulses proportional to the phase difference between them. These UP and DN pulses control the switches in the charge-pump, which converts them into current (I_{DN} or I_{UP}) pulses. The current is then converted to a stable DC voltage by a low pass filter. This DC voltage (V_{tune}) acts as a tuning voltage and adjusts the output of the VCO, such that its phase, when divided by the division factor, is equal to the phase of the reference frequency. In the locked state, the phase difference reaches zero (or a finite value) and the output is a clean single-tone frequency.

The type and order of a synthesizer, which are widely used for PLL nomenclature, is determined by the number of poles at the origin and the total number of poles in the system, respectively. Due to their integrative nature, VCOs have a pole at the origin making all PLLs at least a type-I, first order system. In order to track a frequency step, as required in a frequency synthesizer, another pole at DC is required so that the phase error could be reduced to zero. This pole is accomplished by adding a capacitor (C1 in Fig. 2.7) making the overall PLL a type-II, second order synthesizer. The presence of two poles at the origin causes stability issues, which can be countered by adding a series resistor (R1 in Fig. 2.7) with the capacitor. This introduces a zero in the transfer function hence stabilizing the loop. However, the current pulses generated by the charge pump in every comparison cycle cause a voltage ripple on the VCO control voltage. This ripple deteriorates the spectral purity by modulating the VCO and generating frequency spurs. To overcome this, a second capacitor (C2 in Fig. 2.7) is added to smoothen the control voltage. The addition of this pole categorizes the

PLL as a type-II, third order system. By introducing more poles to further suppress the frequency spurs and noise, higher type and order PLLs are also possible. However, they are rarely used as loop stability becomes a serious concern.

2.4.2 *Frequency Planning*

The frequency planning of the synthesizer is one of the initial steps in system design. Based on the channelization proposals described in Section 2.1, the frequency resolution, which is the minimum frequency step the synthesizer can generate, is determined. The frequency resolution is then used to determine other PLL system parameters in the next section.

The frequency planning is treated in two steps. First, the required LO frequencies for the 40 GHz front-end are listed and next the 60 GHz PLL front-end is analyzed. It is desired that the same reference frequency is utilized for both front-ends as well as to support all HRP and LRP channelization proposals. This eases back-end design of the synthesizer considerably. As evident from Fig. 2.6, the division factor of the prescaler (P) is 2 and 3 for the front-ends, respectively, which changes the overall division ratio while keeping the reference frequency constant. The division ratios are chosen in such a way that N $\times$ P for HRP (2 GHz and 1 GHz) channels is a subset of the division ratio of LRP (500 MHz). Along with 60 GHz, the corresponding frequencies at 40 and 20 GHz are also shown in Table 2.2 to determine the required tuning and locking range of the VCO and prescaler, respectively.

The above table provides a few insights into the requirements of the synthesizer. The LO frequency at 60 GHz spans from 57 to 64 GHz whereas the 40 GHz front-end, which is operating at 2/3 of 60 GHz, requires a locking range from 38 to 42 GHz. The frequency conversion topology involving a tripler requires frequencies from 19 to 21 GHz from the output of the prescaler. For the reference frequency of 300 MHz, the overall division ratio of 127–141 is required to satisfy both LRP and HRP channels. The center frequencies for 1 and 2 GHz channels are identical and only differ in the guard band between two adjacent channels.

The frequency planning of the synthesizer using a 60 GHz front-end is tabulated in Table 2.3. The overall division ratios are higher due to higher VCO frequency and range from 190 to 212. As the center frequencies for the 2 and 1 GHz channel are identical, they are merged in one table. The use of the same reference frequency (300 MHz) results in slightly different center frequencies and bandwidth for the 500 MHz LRP channel as compared to the 40 GHz front-end plan. However, for the proof-of-concept this difference can be ignored. The next section, using these basic requirements further analyzes the synthesizer to determine its complete set of parameters.

Table 2.2 Frequency plan for 40 GHz PLL front-end; for LRP 500 MHz channels (a), for LRP 1 GHz channels (b), and for HRP 2 GHz channels (c)

(a)	For LRP channels (500 MHz)			
Channel number	At 60 GHz	At 40 GHz	At 20 GHz	N × P (for $f_{ref} = 300$ MHz)
C1	57.15	38.10	19.05	127
C2	57.60	38.40	19.20	128
C3	58.05	38.70	19.35	129
C4	58.95	39.30	19.65	131
C5	59.40	39.60	19.80	132
C6	59.85	39.90	19.95	133
C7	60.75	40.50	20.25	135
C8	61.20	40.80	20.40	136
C9	61.65	41.10	20.55	137
C10	62.55	41.70	20.85	139
C11	63.00	42.00	21.00	140
C12	63.45	42.30	21.15	141
(b)	For LRP channels (1 GHz)			
Channel number	At 60 GHz	At 40 GHz	At 20 GHz	N × P (for $f_{ref} = 300$ MHz)
B1	57.60	38.40	19.20	128
B2	59.40	39.60	19.80	132
B3	61.20	40.80	20.40	136
B4	63.00	42.00	21.00	140
(c)	For HRP channels (2 GHz)			
Channel number	At 60 GHz	At 40 GHz	At 20 GHz	N × P (for $f_{ref} = 300$ MHz)
A1	57.60	38.40	19.20	128
A2	59.40	39.60	19.80	132
A3	61.20	40.80	20.40	136
A4	63.00	42.00	21.00	140

2.4.3 Synthesizer Parameters

Phase-lock loops are feedback systems which are inherently non-linear. However, their essential operation can be approximated very well by linear analysis. In such an analysis, the Laplace transform is a valuable tool. The related concept of transfer functions, which describe the s-domain relation between input and output of a linear circuit, is used to analyze the open-loop and closed-loop characteristics of the PLL.

A simplified s-domain representation of the synthesizer is shown in Fig. 2.8. The phase-frequency detector and charge-pump are merged into one block represented by a transfer parameter, K_{PFD} (equal to $I_{cp}/2\pi$). The impedance of the second-order loop filter is shown as Z_{LPF}. The VCO conversion gain, K_{VCO}, represents the sensitivity of VCO frequency with tuning voltage in rad/(s × V). The division

Table 2.3 Frequency plan for 60 GHz PLL front-end

Channel number	For LRP channels (500 MHz)	
	At 60 GHz	N × P (for $f_{ref} = 300$ MHz)
C1	57.00	190
C2	57.60	192
C3	58.20	194
C4	58.80	196
C5	59.40	198
C6	60.00	200
C7	60.60	202
C8	61.20	204
C9	61.80	206
C10	62.40	208
C11	63.00	210
C12	63.60	212
Channel number	For HRP (2 GHz) and LRP (1 GHz)	
	At 60 GHz	N × P (for $f_{ref} = 300$ MHz)
A1, B1	57.60	192
A2, B2	59.40	198
A3, B3	61.20	204
A4, B4	63.00	210

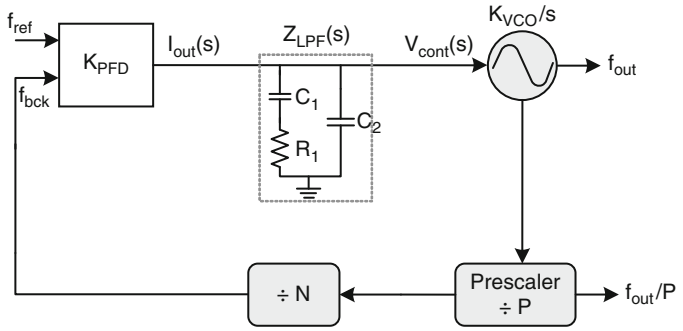

Fig. 2.8 Simplified s-domain representation of the synthesizer

ratio of the prescaler and lower frequency divider chain is represented by P and N, respectively.

The open-loop transfer function of the above synthesizer can be defined as

$$H_{OL}(s) = \frac{K_{PFD}\, K_{VCO}\, Z_{LPF}(s)}{N \cdot P \cdot s} \tag{2.4}$$

which shows a pole at the origin due to the VCO. The over-all loop dynamics are determined by the transfer-function of the loop-filter, which in this case is an

impedance function, as it converts the charge-pump current to a tuning voltage for the VCO. $Z_{LPF}(s)$ is expressed as

$$Z_{LPF}(s) = \frac{1 + sR_1C_1}{s(sR_1C_1C_2 + C_1 + C_2)} \tag{2.5}$$

Equation (2.5) shows the first loop-filter pole at $\omega_{p1} = 0$ and the zero at

$$\omega_z = 1/R_1C_1 \tag{2.6}$$

The two poles at the origin (first one due to VCO and second one, ω_{p1}) can render the loop unstable as the phase-margin is zero. The addition of ω_z stabilizes the loop and proper positioning can provide sufficient phase-margin to ensure loop stability as will be discussed shortly. To obtain a meaningful expression for the second pole, which relates it with ω_z, (2.5) is re-arranged by introducing a variable $m = (C_1 + C_2)/C_2$ as

$$Z_{LPF}(s) = R_1 \frac{1 + s/\omega_z}{s\left(1 + \frac{s}{\frac{C_1+C_2}{R_1C_1C_2}}\right)/\omega_z} \frac{m-1}{m} \tag{2.7}$$

which shows the second loop-filter pole at

$$\omega_{p2} = \frac{1}{R_1C_1}\frac{C_1 + C_2}{C_2} = m\omega_z \tag{2.8}$$

and thus simplifying $Z_{LPF}(s)$ as

$$Z_{LPF}(s) = R_1 \frac{1 + s/\omega_z}{s\left(1 + \frac{s}{\omega_{p2}}\right)/\omega_z} \frac{m-1}{m} \tag{2.9}$$

Using (2.9), the open-loop transfer function of (2.4) can be re-written as

$$H_{OL}(s) = A \frac{1 + s/\omega_z}{s^2\left(1 + \frac{s}{\omega_{p2}}\right)/\omega_z} \frac{m-1}{m} \tag{2.10}$$

where A is

$$A = \frac{K_{PFD}\, K_{VCO}\, R_1}{N \cdot P} \tag{2.11}$$

The magnitude and phase of the open-loop transfer function can be drawn in a Bode plot to get insight into poles and zero positions and conditions for stability of

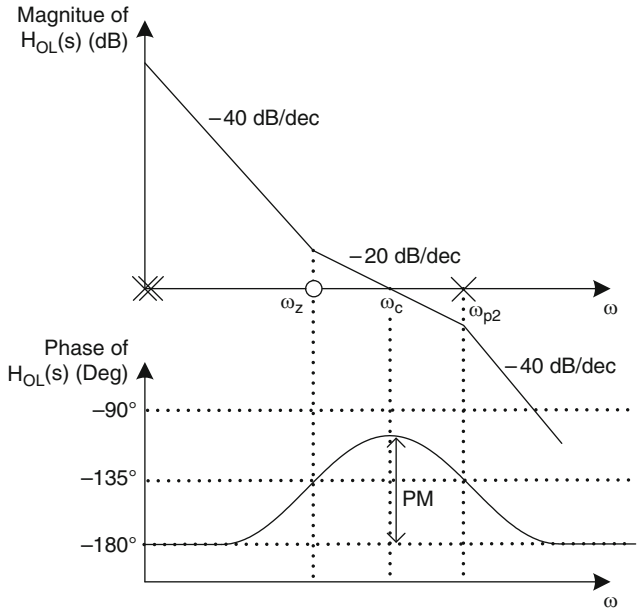

Fig. 2.9 Open-loop magnitude and phase response

the loop. This is illustrated in Fig. 2.9. The zero at ω_z decreases the slope from 40 to 20 dB/dec and more importantly increases the phase from $-180°$. The value of the phase, where magnitude is unity or 0-dB, is called the phase margin (PM). The frequency of the cross-over point is the loop bandwidth of the PLL denoted by ω_c. The latter is calculated by equating the magnitude of (2.10) to unity which yields

$$\omega_c = A\,\frac{m-1}{m}\,\frac{\cos(\Phi_{p2})}{\sin(\Phi_z)} \tag{2.12}$$

where $\Phi_z = \tan^{-1}(\omega_c/\omega_z)$ and $\Phi_{p2} = \tan^{-1}(\omega_c/\omega_{p2})$. The phase-margin can be expressed as

$$\Phi_m = -180° + \Phi_z - \Phi_{p2} = 180° + \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \tag{2.13}$$

Ideally, the phase-margin should be maximized to ensure loop stability and also to cater for variations in resistance and capacitance values which determine the poles and zero positions. The maximum possible phase-margin can be found by differentiating (2.13) and solving for ω_c as

$$(\omega_c)_{for\ \max\ PM} = \sqrt{\omega_z\,\omega_{p2}} = \sqrt{m}\,\omega_z \tag{2.14}$$

Substituting ω_c in (2.13) yields the maximum phase-margin as

$$(\Phi_m)_{\max} = -180^\circ + \tan^{-1}\sqrt{\frac{\omega_{p2}}{\omega_z}} - \tan^{-1}\sqrt{\frac{\omega_z}{\omega_{p2}}} = \tan^{-1}\frac{(m-1)}{2\sqrt{m}} \tag{2.15}$$

Equations (2.14) and (2.15) show that, firstly, for optimal stability (maximum PM), the unity gain crossover point should be the geometric mean of the zero and second pole as this is the position where the phase is farthest from 180°. Secondly, the maximum phase-margin is exclusively determined by the capacitor ratio (m) which is also the ratio of the second pole (ω_{p2}) and zero (ω_z). Figure 2.10 shows the phase margin for different values of m. It is noticed that due to the arc-tangent function the curve is asymptotic to 90°.

Using $\Phi_z = \tan^{-1}(\sqrt{m})$ and $\Phi_{p2} = \tan^{-1}(1/\sqrt{m})$, it is observed that $\sin(\Phi_z) = \cos(\Phi_{p2})$ which simplifies (2.12) to

$$\omega_c = A\,\frac{m-1}{m} = \frac{K_{PFD}\,K_{VCO}\,R_1}{N\cdot P}\,\frac{m-1}{m} = \frac{K_{PFD}\,K_{VCO}\,R_1}{N\cdot P}\,\frac{C_1}{C_1+C_2} \tag{2.16}$$

The closed-loop transfer function of the type-II, third-order PLL is given by

$$H_{CL}(s) = \frac{1+s/\omega_z}{1+\frac{s}{\omega_z}+\frac{s^2}{K\omega_z\frac{m-1}{m}}\left(1+\frac{s}{\omega_{p2}}\right)} \tag{2.17}$$

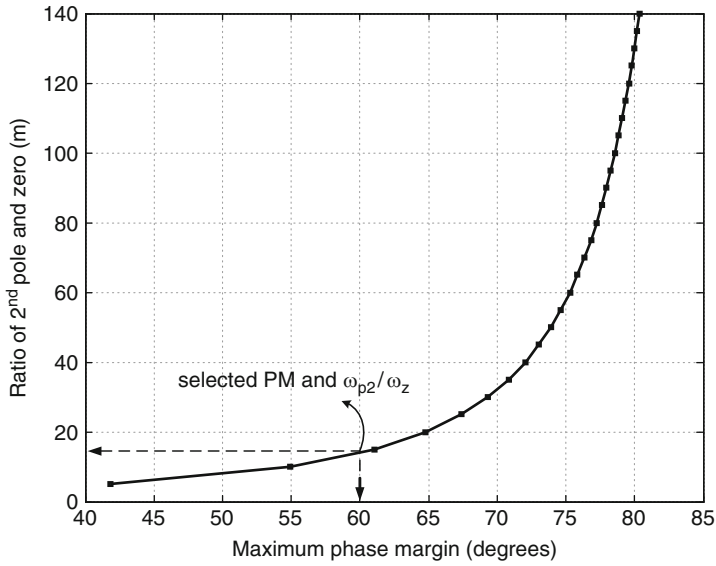

Fig. 2.10 Maximum phase margin vs. ratio of second pole (ω_{p2}) and zero (ω_z)

The frequency planning covered in the previous section and the above mentioned expressions will be employed to determine the PLL parameters next:

- The specified output frequencies in Tables 2.2 and 2.3 define the required tuning range of the VCOs and this, together with the supply voltage determines the associated gain, K_{VCO}. For the 40 GHz front-end the VCO requires a tuning range from 38 to 42.3 GHz. Supposing a VCO tuning voltage of 1.2 V (nominal supply for sub-nanometer CMOS technologies), the resulting VCO gain is equal to $K_{VCO} = 2\pi \times 3.58$ G rad/s $\times$ V. On the other hand, for the 60 GHz front-end, the required VCO tuning range is 57–63.6 GHz and the $K_{VCO} = 2\pi \times 5.5$ G rad/s $\times$ V. These parameters also require some safety margins to cater for PVT variations and are included during circuit design.
- The reference frequency for both front-ends is identical and equal to $f_{ref} = 300$ MHz. The resulting division ratio range is $N \times P = 127$–141 for the 40 GHz front-end and $N \times P = 190$–212 for the 60 GHz front-end.
- The choice of the loop-bandwidth (ω_c) is an important step for the overall PLL design and a number of considerations have to be analyzed. Firstly, settling time which is defined as the time required by the loop to switch from one channel to another, is dictated by the chosen loop bandwidth. Secondly, to ensure loop stability ω_c (or f_c) should be a fraction of the reference frequency. This is treated in sufficient detail in [26] which estimates a condition of $f_{ref}/10 > f_c$ for loop stability. Lastly, ω_c affects the noise transfer characteristic of the PLL and defines the "knee" in the overall phase noise curve. This will be discussed in Section 2.6.

Having selected a $f_{ref} = 300$ MHz, the above mentioned stability bound is satisfied (with some margin) by selecting a loop bandwidth of $f_c = 4$ MHz. This value also results in reasonably valued loop filter components which can be integrated on-chip. There is no specification for settling time proposed in the current standard however the chosen f_c results in a settling time of $\sim$1 µs.

- The next step is to determine the frequency of the zero (ω_z) and second pole (ω_{p2}). To achieve a phase margin of 60° the capacitance ratio m must equal 13.93 (see Fig. 2.10). The optimal position of the zero and pole can be calculated using (2.8) and (2.14) which show that ω_c should be the geometric mean of ω_z and ω_{p2}, i.e.

$$f_z = \frac{f_c}{\sqrt{m}} = 1.072\text{MHz} \quad \text{and} \quad f_{p2} = \sqrt{m}\, f_c = 14.93\text{MHz} \tag{2.18}$$

- Using (2.16) and a PFD gain of 500 µA/2π, resistor and capacitor values of the loop filter can be determined. The difference in VCO gain and division ratios for the two front-ends could lead to different loop filter values. However, the ratio of

Table 2.4 Summary of calculated PLL parameters

40 GHz front-end	VCO tuning range	38–42.3 GHz
	K_{VCO}	3.58 GHz/V
	Division ratio	127–141
60 GHz front-end	VCO tuning range	57–63.6 GHz
	K_{VCO}	5.5 GHz/V
	Divide ratio	190–212
Reference frequency		300 MHz
Loop bandwidth		4 MHz
Charge-pump current		500 μA
Settling time		∼1 μs
Second-order loop filter	R1	2 kΩ
	C1	74.2 pF
	C2	5.74 pF

selected K_{vco} and average division ratio in (2.16) closely match. Therefore, the overall calculations are unaffected and the loop filter does not require different resistance and capacitance for the two front-ends. This re-usability of the area consuming LPF saves considerable silicon area.

The calculated resistance R1 = 2 kΩ and (2.6) yields for the first capacitor C1 = 74.2 pF. The last loop filter component C2 = 5.74 pF is calculated using the capacitance ratio term, m.

The key PLL parameters calculated above are summarized in Table 2.4.

2.5 System Simulations

PLL based frequency synthesizers consist of components operating at vastly different frequencies. The VCO and prescaler, operating at the highest frequencies, require a high numerical sampling rate in the simulations whereas the low frequency components like PFD have large time constants. Consequently, the simulation of such systems is not trivial as few micro-seconds transient simulation coupled with a small time step means millions of time points are required. Therefore, prior to full-blown circuit level simulations, system level simulations based on behavior models are often adopted. These simulations provide a first insight into the overall system operation and the interaction of different components with each other.

Agilent's Advanced Design System (ADS) provides an adequate tool-box for PLL related simulations. The loop's AC response to extract stability information like phase margin, dynamic behavior to obtain settling time, and noise performance are all possible using this tool. A basic simulation environment is depicted in Fig. 2.11. The LPF block is custom-made based on the second order loop filter equations. The divider is used to step the division ratio and VCO output is demodulated using the *FM_Demod* block to obtain the settling time results. A similar setup, with a difference of the loop being opened, is simulated to

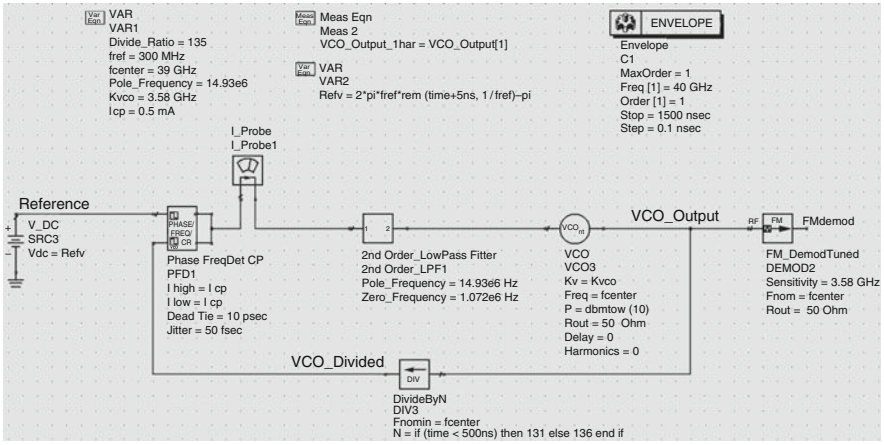

Fig. 2.11 ADS basic simulation environment

acquire open-loop gain and phase response of the PLL. The PFD and charge pump are merged into one block and characterized by relevant parameters like I_{cp}, dead-zone time and timing jitter. The dead-zone phenomenon is an undesired characteristic of PFDs which refers to its inability to track the phase difference between the two input signals. In such a case, the output charge pump current is zero and the spurious tones appear at the VCO output un-attenuated. The timing jitter parameter models the noise in the charge pump current which corresponds to jitter at the PFD input. These two variables are assigned simulated values based on separate PFD and charge pump simulations in ADS. The current probe shows the charge pump current being pumped into the loop filter to move the synthesizer towards lock.

The open loop gain and phase response of the synthesizer is shown in Fig. 2.12. The gain curve reflects the system pole positions. The starting slope is −40 dB/dec due to two poles at the origin and reduces to −20 dB/dec due to the introduction of stabilizing zero (ω_z) at 1.072 MHz. The high frequency pole (ω_{p2}) at 14.93 MHz modifies the slope again to −40 dB/dec. The phase at 0-dB cross-over point is −120° showing that phase margin is 60° as desired. To estimate the settling time, the division ratio is first changed to 131 and then incremented to 136. This corresponds to a 500 MHz and 2 GHz frequency jump at 60 GHz, respectively. The settling time obtained is about 1 μs as shown in Fig. 2.13.

The ideal output of a frequency synthesizer is a pure sinusoidal waveform. However, just like any other integrated electronic system, non-idealities such as noise degrade the spectrum purity of the output signal. This can potentially result (among other negative impacts) in lower sensitivity, poor blocking performance on the receiver side, and increased spectral emissions on the transmitter side. The output of a typical synthesizer can be expressed as

$$v_{out}(t) = V_0 \cos\left(f_{LO}t + \Phi_p(t)\right) \tag{2.19}$$

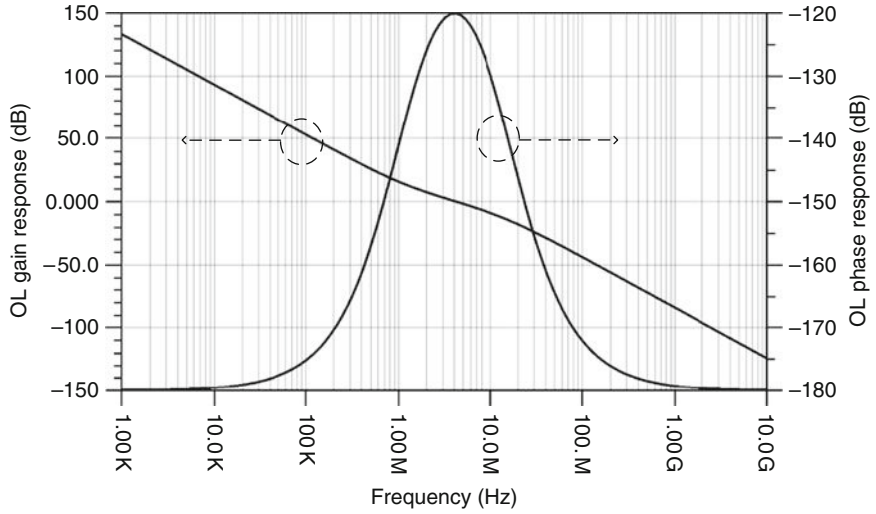

Fig. 2.12 Open-loop gain and phase response of PLL

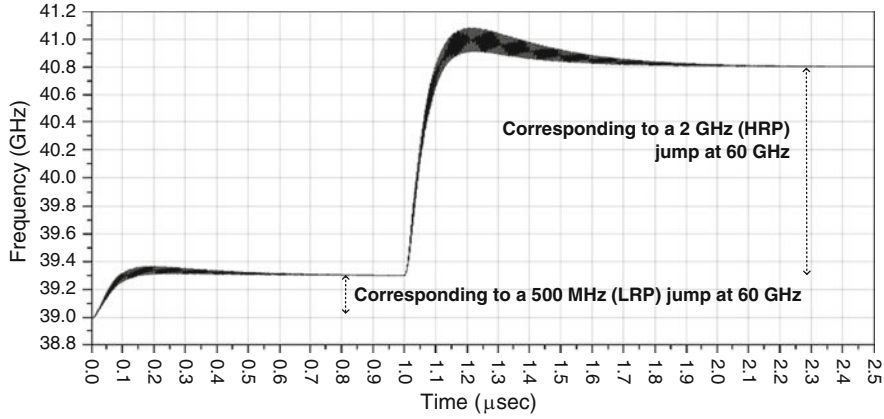

Fig. 2.13 Settling time corresponding to a 500 MHz and 2 GHz frequency jump

where $f_{LO}t$ is the desired phase of the output and $\Phi_p(t)$ models the phase fluctuation in the PLL output. Noise generated by phase fluctuations of particular interest for synthesizer performance. These fluctuations can be categorized into periodic and random variations as

$$\Phi_p(t) = \Delta\Phi_p \ \sin(2\pi f_s t) + \varphi(t) \tag{2.20}$$

The first term represents the periodic phase variations which produce discrete spurious tones at an offset frequency f_s from the carrier frequency f_{LO}. The level of

these spurs should be as low as possible as compared to the carrier to avoid up- or down-conversion to the desired frequency band after LO mixing. The second term represents the random phase variation and produces phase noise, which is a measure of how much the output diverges from a pure tone in the frequency domain.

The overall phase noise characteristic of the synthesizer is formed by all the different circuits and components that make up the control loop. The noise contribution can be understood by Fig. 2.14 (slopes exaggerated for identification):

The noise contributions from the low frequency components such as the loop filter, PFD and charge pump are shaped by a low-pass transfer function when it appears at the synthesizer output whereas the VCO phase noise experiences a high-pass transfer function as it appears at the output of the synthesizer. The corner frequency between these two transitions is determined by the loop bandwidth, f_c. Therefore, as depicted by Fig. 2.14, the in-band phase noise is dominated by all synthesizer components other than VCO and the out-of-band phase noise follows the VCO phase noise curve. It is evident that by increasing the loop bandwidth more VCO noise can be filtered; however, it cannot be arbitrarily increased due to stability issues as mentioned in Section 2.4.3.

To estimate phase noise performance of the synthesizer in ADS, typical noise contributions of individual components are used. Figure 2.15 shows the overall synthesizer phase noise as well as contributions from individual components such as VCO, PFD and CP. The noise of feedback divider and loop filter are not dominant, therefore omitted for clarity. The loop bandwidth of 4 MHz forms the "knee" in the phase noise curve. The in-band phase noise, say at 100 kHz is dominated by PFD and charge pump and is about −110 dBc/Hz whereas out-of-band noise, say at 30 MHz is dominated by the VCO and is −128 dBc/Hz. These values provide a first estimate about the expected phase noise performance. However, the simulation does not include all noise mechanisms which are present at circuit level.

Similar simulations are carried out with a 60 GHz front-end by replacing the VCO and modifying the overall division ratio. The loop dynamic performance including phase margin and settling time yield similar results because the loop filter remains un-changed for both designs as explained in Section 2.4.3. On the other

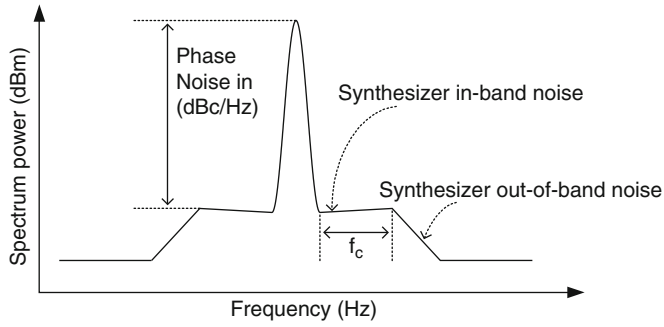

Fig. 2.14 Typical phase noise spectral plot of a synthesizer

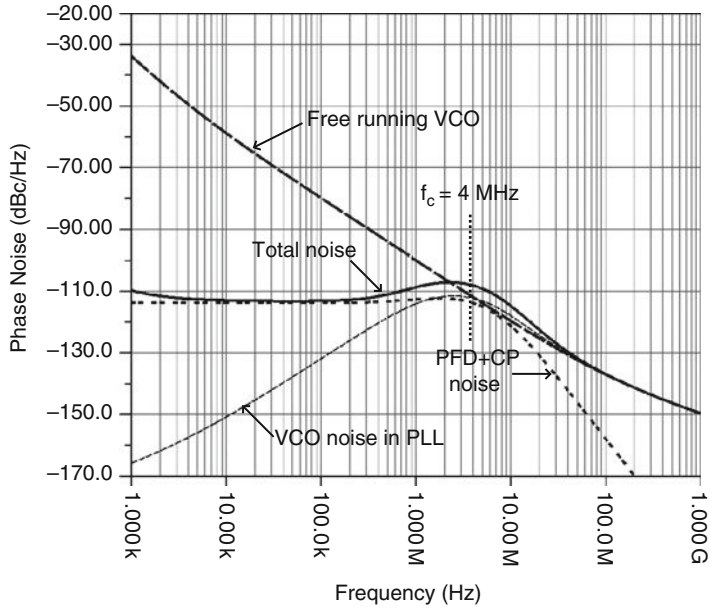

Fig. 2.15 ADS simulation for synthesizer and components phase noise

hand, the phase noise is degraded. Firstly, due to higher division ratio the in-band phase noise increases by 20 log(ΔN), where ΔN is the change in average division ratio while moving from a 40- to a 60 GHz front-end [27]. Secondly, the VCO at 60 GHz has a worse phase noise as compared to its 40 GHz counter-part, so the out-of-band phase noise is also higher for this front-end.

2.6 Target Specifications

Utilizing the calculated parameters and system simulations of the synthesizer in the preceding two sections, performance specifications for the system as well as components are summarized in this section.

The overall synthesizer specifications mainly include the locking range, phase noise and settling time. The VCO for the 40 GHz front-end utilizes a divide-by-2 prescaler. Due to the division the phase noise should be 6 dB better than the VCO phase noise. Similarly, in the 60 GHz front-end the divide-by-3 prescaler should have 9.5 dB better phase noise than the VCO. The envisioned dual-mode prescaler is expected to cover the locking range of both divide-by-2 and divide-by-3 prescalers based on the input frequency. The feedback divider chain or the feedback mixer translates the output frequency of the prescaler to around 300 MHz for

Table 2.5 Target specifications of synthesizer and components

Overall frequency synthesizer	Locking range	38–42.3 and 57–63.6 GHz
	Settling time	~1 μs
	In-band phase noise	−100 dBc/Hz
	Out-of-band phase noise	−110 dBc/Hz
40 GHz VCO	Tuning range	38–42.3 GHz
	Phase noise	−100 dBc/Hz at 1 MHz
Prescaler divide-by-2	Locking range	38–42.3 GHz
	Phase noise	<−106 dBc/Hz at 1 MHz
60 GHz VCO	Tuning range	57–63.6 GHz
	Phase noise	−90 dBc/Hz at 1 MHz
Prescaler divide-by-3	Locking range	57–63.6 GHz
	Phase noise	<−100 dBc/Hz at 1 MHz
Dual-mode prescaler	Locking range	38–42.3 and 57–63.6 GHz
	Phase noise	<−100 dBc/Hz at 1 MHz
Feedback divider chain	Division ratio (40 GHz front-end)	127–141
	Division ratio (60 GHz front-end)	190–212
Feedback mixer	RF frequency	19–21 GHz
	IF frequency	~300 MHz
Phase frequency detector	Comparison frequency	~300 MHz
	Dead-zone	Zero

comparison with the reference frequency in the phase frequency detector. The main specifications are enlisted in Table 2.5.

2.7 Summary

This chapter lays down the foundation for circuit design of the synthesizer in subsequent chapters. After a brief discussion of different standardization efforts for the 60 GHz frequency band, IEEE 802.15.3c is discussed in detail. The frequency channelization proposals of this standard include 2 GHz HRP channels for data intensive applications such as live video streaming and downloads and 1 GHz and 500 MHz LRP channels for moderate and low data rate applications, respectively. In order to work-around some of the 60 GHz circuit design challenges, a variety of alternative frequency conversion techniques are possible which have been presented in Section 2.2. With the aim of supporting a number of these frequency conversion techniques, a flexible synthesizer architecture has been proposed. While re-using the same back-end the synthesizer will support the sliding-IF topology, as well as direct conversion with and without a frequency tripler by using dual-band or switchable front-ends based on 40 and 60 GHz VCOs.

A brief overview of PLL basics is included before frequency planning of the synthesizer is presented. The required LO frequencies and division ratios for both front-ends are enlisted in Section 2.4.2. The reference frequency is identical for both front-ends and division ratios are chosen in a way that the required loop filter

remains the same, thus saving considerable silicon area. The calculation of synthesizer parameters is treated in detail followed by system level simulations in ADS. These simulations provide an overview of the dynamic performance of the synthesizer and assist in laying down the target specifications of the synthesizer in Section 2.6.

Chapter 3
Layout and Measurements at mm-Wave Frequencies

Abstract Millimeter wave layout and measurements pose serious challenges during the IC design cycle. Therefore, this chapter is dedicated to discuss the various issues encountered and proposes solutions for them. The first part of the chapter elaborates the impact of parasitics, layout mismatch, substrate losses and shielding whereas the second part discusses the measurement issues like calibration, de-embedding, stability and repeatability.

Keywords Millimeter wave layout · RF measurements · Parasitics · Substrate losses · Grounding · Shielding · Calibration · De-embedding

Integrated circuits at millimeter wave frequencies, in addition to circuit design challenges, pose some extra complexities and uncertainties. These are related firstly, to the layout and floor-plan of components, and secondly, to the measurement of these circuits. Both these issues are under-researched particularly at mm-wave frequencies and it is difficult to locate a "one-stop" book tackling these topics. Furthermore, unlike digital design, in which layout is generated automatically (in most cases) based on well defined rules, analog and RF requires custom layout for all components. There are "no rules" for floor-planning or layouting and only some general guidelines are followed, the affect of which is generally not characterized or studied adequately.

The substantial effect of layout on circuit performance and the challenge in carrying accurate measurements necessitate the need for analysis and identification of potential problems and their solutions during the design process. In this book, solutions to some of these problems have been widely utilized in designs elaborated in the subsequent chapters. Therefore, to provide a common-ground, this chapter is dedicated to address the layout and measurement aspects at mm-wave frequencies. Section 3.1 discusses various layout issues and the proposed solutions. The undesired inductance and capacitance or parasitics emanating from the layout are of the same order as the required passive values at these frequencies. Consequently, their effect is more significant than at lower frequencies and needs to be carefully accounted for. Mismatches (phase and amplitude) due to layout asymmetry and

H.M. Cheema et al., *60-GHz CMOS Phase-Locked Loops*,
DOI 10.1007/978-90-481-9280-9_3,

different device orientation also become visible. Owing to low-resistivity, CMOS substrates incur losses for passive structures such as inductors, transformers and transmission lines, degrading their high frequency performance. Furthermore, cross-talk between RF interconnects in close proximity deteriorates the spectral purity of signals and requires isolation and shielding from each other. Variation in ground potential in different parts of the integrated circuit generates erroneous voltage levels and innovative grounding techniques are required to achieve a common reference voltage all over the chip. As will be discussed, the solutions to these problems are sometimes contradictory and the designer has to identify the most dominant one based on circuit application and frequency and find the best compromise. Section 3.2 discusses measurement related challenges for mm-wave frequencies. Firstly, dedicated instrumentation is a pre-requisite, specifically for high frequency measurements, as indirect methods can yield inaccurate results. Secondly, the contribution of external elements like cables, probes and bond-pads has to be subtracted from the measurement data for which calibration and de-embedding techniques are employed. These techniques pose a number of challenges at mm-wave frequencies which require careful consideration and are discussed in Section 3.2.2. Lastly, the variation of measurements due to minor physical changes in the setup become more visible at these frequencies which may rise stability and repeatability issues. These are discussed in Section 3.2.3.

3.1 Layout Problems and Solutions

The intermediate step between schematic-level design and actual fabrication of integrated circuits is the layout of active and passive components. Layouting primarily involves connecting these components using conductive metal called interconnect. The low frequency circuit theory techniques (KCL, KVL) treats the circuit elements and interconnects as lumped elements which is only valid if the dimensions of the circuit are small compared to the shortest wavelength of interest. This is because variations in the resistance (R), inductance (L) and capacitance (C) values between separated points in the circuit are then negligible. If, however, the wavelength becomes comparable to the circuit dimensions, the assumption does not hold and distributed effects begin to dominate. The R, L and C values cannot always be localized, as at a given instant, the voltage (or current) at one point in the circuit maybe passing through its maximum value, while at another point it is zero. A generally accepted rule-of-thumb between these two regimes is that if the circuit dimensions are smaller than $\lambda/10$, traditional lumped analysis can be used and if comparable or larger than $\lambda/10$, distributed analysis has to be adopted.

In order to obtain numerical information related to the above constraint, the effective wavelength of 60 GHz signals on chip can be determined. The wavelength of a sinusoid in free space is given by

$$\lambda_0 = \frac{c}{f} \tag{3.1}$$

where c is the velocity of light in free space (3×10^8 m/s), f is the operation frequency and λ_0 is the free space wavelength. In a medium other than air, the wavelength is reduced by square-root of its dielectric constant (ε_R), as the speed of propagation is also reduced by the same proportion. So, the effective wavelength (λ) for a sinusoid in a dielectric other than air is given by

$$\lambda = \frac{\lambda_0}{\sqrt{\varepsilon_R}} = \frac{c}{f\sqrt{\varepsilon_R}} \tag{3.2}$$

In case of silicon, the dielectric constant is 11.7 and using a frequency of 60 GHz, the resulting wavelength of a sinusoid on chip is $\lambda = 1.46$ mm.[1] This reflects the first major problem with mm-wave layout as $\lambda/10$ factor is equal to 146 μm which can potentially be in the same order as the circuit dimensions. This means that firstly, RF interconnects carrying the high frequency signals should be as short as possible, secondly, the long interconnects should be realized as transmission lines (T-lines) having a controlled impedance and termination, and thirdly, the interconnects in the vicinity of above dimensions have to be treated in a distributed fashion involving meticulous calculations or electromagnetic (EM) simulations.

The guideline of 146 μm only provides the first bound. However, in reality the cut-off is application and frequency dependent. For instance, distributed analysis and EM simulations become necessary even for RF interconnects above 10 μm for 60 GHz circuit design. This is because the un-wanted inductance and capacitance of interconnects, active and passive devices, generally named as "parasitics" are of the same order as the required L and C at mm-wave frequencies. Therefore, if un-accounted, these parasitic components can result in severe off-target results and in worse case, failure of an integrated circuit. To get an idea, let us consider an example of an LC oscillator. Fixing the inductance to a typical value of 200 pH, the required capacitance is plotted as a function of frequency from 30 to 100 GHz in Fig. 3.1. At 40 and 60 GHz, the capacitance is 80 and 35 fF, respectively. These values, already very small, should still accommodate the varactor as well as parasitic capacitances generating from active and passive devices and the interconnects. Similarly, fixing the capacitance to 0.3 pF the inductance at 60 GHz is only 20 pH which can easily be affected by interconnect inductance resulting in a shift of the oscillation frequency. Therefore, these parasitics should be carefully accounted for, during the design and will be elaborated further in subsequent sections.

3.1.1 Impact of Parasitics

The importance of parasitics is evident from the discussion in the preceding section. The next question is how to estimate them accurately? To start off, there is no

[1] In case of using silicon dioxide SiO_2 as reference, the dielectric constant is 3.9 and corresponding wavelength is 2.5 mm.

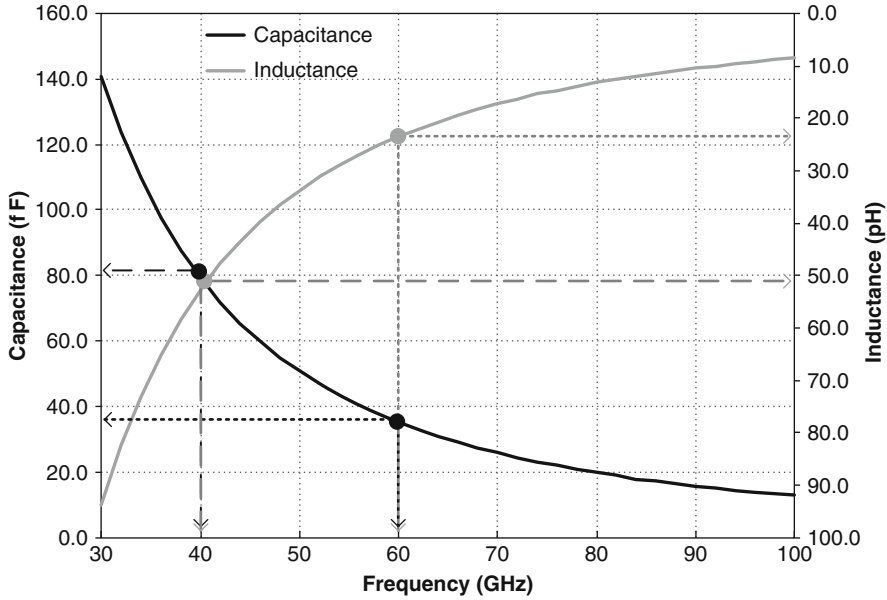

Fig. 3.1 Capacitance (with L = 200 pH) and inductance (with C = 0.3 pF) required for an oscillator as a function of frequency

one-tool which can do-it-all. Therefore, a number of different simulation and extraction tools are utilized to accomplish the task. A typical IC design flow is shown in Fig. 3.2. It is to be noted, as will be explained shortly, that the steps inside the dashed box are more critical in a mm-wave design flow as compared to a low frequency design. In case the post-layout simulations, which usually include RC extraction from one tool and inductance extraction from EM-solvers, do not meet the required specifications, the layout has to be modified and subsequently the extraction has to be repeated. This dictates an iterative (and time consuming) procedure until the specifications are met successfully.

The term "the smaller, the better" summarizes the best-practice for mm-wave layout. Arbitrary floor planning resulting in long interconnects can not only result in off-target results but also increase the design and simulation time in estimating its parasitics. Another issue lies in the accuracy of the extraction results. The parasitic RC estimation of devices as well as interconnects is usually carried out in "Cadence Design Environment" whereas, for inductance estimation of critical RF interconnects, both 2.5-D EM solvers such as ADS Momentum and Sonnet or 3-D solvers like CST Microwave Studio are employed. The extraction tools do not offer "pin-point" accuracy and use a variety of tools (sometimes incompatible and requiring approximation to be used) increases the uncertainty of the results. Therefore, a dry-run of critical components may be needed to get "a feel" of the technology and accuracy of extraction tools at mm-wave frequencies.

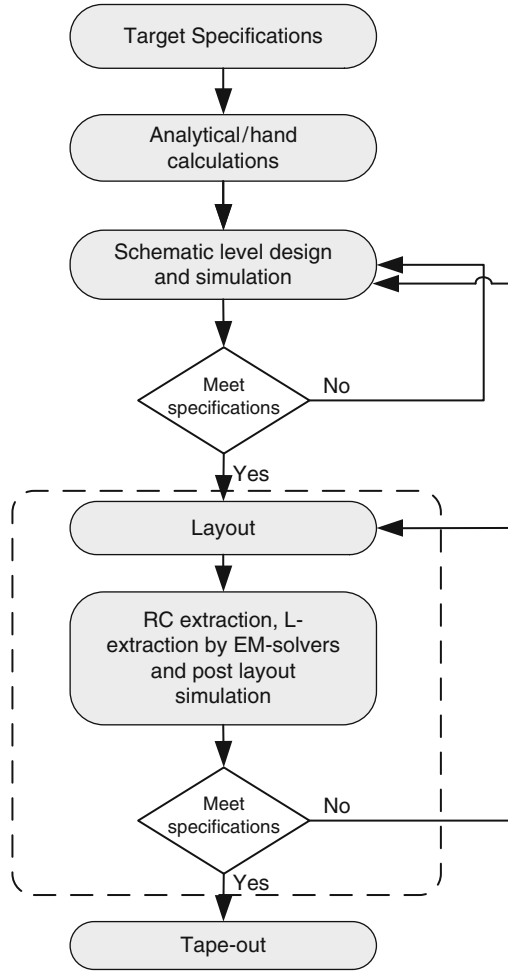

Fig. 3.2 A typical IC-design flow with an iterative layout and extraction cycle

Current sub-nanometer CMOS technologies offer multiple conductive metal layers (together called stack) which can range from three to ten in number. The thickness of these layers can be different from each other due to which the resulting inductance is also different. The lowest metal is usually the thinnest and top-metal the thickest. At lower frequencies the interconnect using these metal layers is not critical; however, at mm-wave frequencies the inductance of these lines becomes an important factor. As an example, for a CMOS 65 nm technology using a six layer metal stack, the inductance of a 2 μm wide line is plotted in Fig. 3.3 for lengths between 5 and 120 μm for the top metal (Me6) and bottom metal (Me1). It can be seen that the inductance for an interconnect as small as 5 μm is 6 pH. If this inductance is unaccounted in a 60 GHz oscillator it can shift the center frequency by

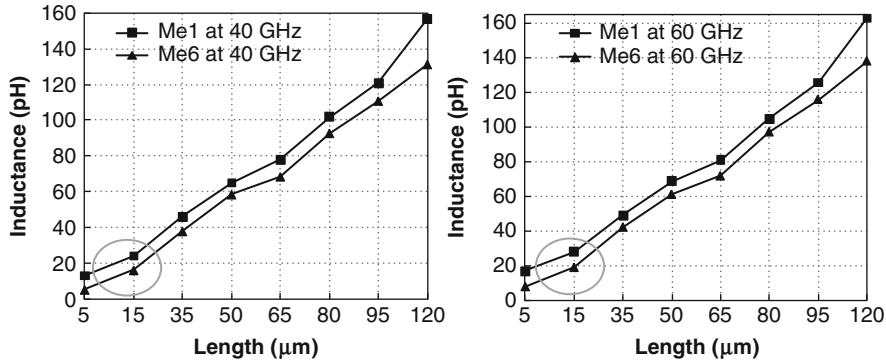

Fig. 3.3 Interconnect inductance for lowest metal (Me1) and highest metal (Me6) as a function of length at 40 GHz (*left*) and 60 GHz (*right*)

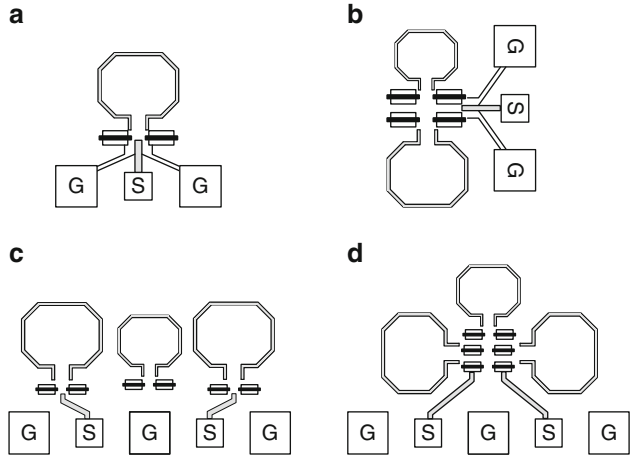

Fig. 3.4 Floor-planning of a VCO (**a**), VCO and prescaler with single-ended output (**b**), VCO and prescaler requiring long interconnects (**c**), and VCO and prescaler with short interconnects (**d**)

2.25 GHz (assuming a total capacitance of 100 fF). This confirms the necessity of accurately estimating parasitics in a mm-wave layout.

In order to keep interconnects short, the floor planning of components need special attention. In this work, interconnects of the synthesizer front-end are most critical as it operates at the highest frequency. Therefore, the floor-planning of the VCO and prescaler is discussed next. A typical LC-VCO consists of at least one inductor and some active devices such as transistors and varactors. To achieve short interconnects, the latter should be placed very close to the inductor terminals (see Fig. 3.4a). The VCO output which needs to be measured by using a bond-pad is unavoidably long, so transmission lines whose impedance can be well controlled is employed for such connections.

There are a number of prescaler circuits possible for mm-wave synthesizers, one of which is based on injection locking (discussed in Chapter 4). Such a prescaler requires at least one inductor for a non-quadrature output and two for quadrature outputs. The former case is depicted in Fig. 3.4b along with the VCO. The two inductors are placed opposite to each other and the core active circuit is placed in between their terminals. The output is drawn from the right (or left) of the front-end layout. In case of quadrature outputs two possible arrangements are depicted in the Fig. 3.4c and d. The former offers short output lines to the pads. However, due to the side-by-side placement of inductors, the interconnections are long. On the other hand the floor-plan of Fig. 3.4d keeps the interconnects very short and should be preferred over the other arrangement.

3.1.2 Mismatch Due to Layout Asymmetry and Device Orientation

The small dimensions of mm-wave layouts and considerable affect of parasitics imply that the symmetry of the high frequency interconnects and orientation of devices also become critical, especially in circuits requiring phase accuracy. Examples of such circuits could be coupled VCOs, frequency dividers providing quadrature outputs, poly-phase filters etc. The symmetry and length of the interconnect is linked to the orientation and arrangement of devices. The requirement of symmetrical interconnect is, sometimes, in contradiction with the guide-line of keeping it as short as possible mentioned in the previous section. In such a scenario, an optimal trade-off is likely to be made.

An example is shown is Fig. 3.5 which shows two possible arrangements of active devices of an actively coupled I-Q VCO [28]. The layout in Fig. 3.5a is

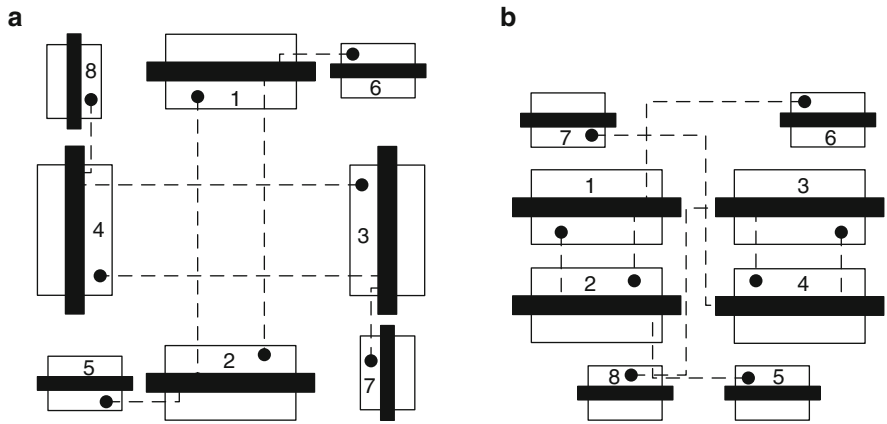

Fig. 3.5 Layout comparison between symmetric but long interconnects with transistor orientation mismatch (**a**), and unsymmetrical layout but short interconnects with identical transistor orientation (**b**)

perfectly symmetrical. However, the interconnects between the devices 1 and 4 are long and, in addition, the orientation of devices is not identical which gives rise to larger mismatch during fabrication (∼10%). The arrangement in Fig. 3.5b has shorter interconnects between 1 and 4, but they are not symmetrical. Furthermore, the orientation of transistors is identical in this approach which only results in a relative mismatch during lithography (∼2%). Therefore, based on the circuit requirements, a particular layout arrangement has to be chosen for mm-wave designs.

In a frequency synthesizer, the layout symmetry is also important for low frequency components such as phase frequency detector and charge pump. This is because they consist of two identical paths (or sub-circuits), one for the reference frequency and the other for the feedback signal. The layout mismatches in these components can increase (or decrease) the delay in one of the two paths, potentially resulting in incorrect operation and degrading the spectral purity of the synthesizer's output as well.

3.1.3 Substrate Losses

Current CMOS technologies typically offer low to moderate resistive substrates with $\rho = 1-10$ Ω-cm (even lower for older technologies). Such conductive substrates provide low impedance paths for RF signals to propagate through, especially in case of passive elements such as on-chip inductors and transformers. The time-varying magnetic fields of the passive element induce an electromotive force (EMF) in the substrate leading to current flow. These currents, called eddy currents, cause power loss which appears as an effective increase in the series resistance of inductors.

For frequencies lower than 10 GHz and moderately conductive substrates, the induced eddy currents are small and can be neglected. However, this is not the case as the operation frequency moves into the mm-wave regime. Consequently, realizing high quality-factor (Q) inductors, which is already a challenge at frequencies in excess of 10 GHz, becomes even more demanding due to the substrate induced losses.

A number of solutions can be adopted to address this loss mechanism:

- High resistivity substrates with ∼10 kΩ-cm can be used to decrease the induced currents. Un-doped silicon or insulators such as sapphire have been used in Silicon-on-Insulator (SOI) technologies to achieve high resistivity. Using SOI technologies, high-Q passives have been demonstrated. However, this requires extra processing steps during lithography, increasing the implementation costs.
- The second method is to shield the passive element from the substrate by introducing a ground shield between them. The shield can be constructed with polysilicon or a metal layer farthest in the stack from the inductor metal layer. The shape of the ground shield is an important factor in the reduction of losses. Induced currents in the shield flow in a direction as to reduce the overall

magnetic field and therefore inductance. A solid ground shield allows eddy currents to loop over a large area, creating a larger magnetic field cancellation. Therefore, small discontinuities (patterns) in the ground shield are introduced to reduce these eddy current loops to smaller area thereby lowering the cancellation effect. In addition, there is less magnetic field penetration into the substrate resulting in reduction of substrate losses. A few examples of patterned ground shields are shown in Fig. 3.6a–c.

The drawback of the shield method is the possible reduction of self-resonance frequency (FSR) of the inductor caused by the increased capacitance. One way to mitigate this issue is to use the metal layer (as shield) which is most far from the inductor metal layer.

- An alternative to the shield structure is to introduce a "ground ring" which surrounds the passive element as shown in Fig. 3.6d. This ring captures most of the fringing fields from reaching the substrate, thereby reducing the associated losses. As the ring does not form a closed loop around the inductor, it does not affect the magnetic field of the latter significantly.

In this work, the latter two methods are widely employed to achieve isolation from substrate losses of the inductors employed in VCO and prescaler circuits.

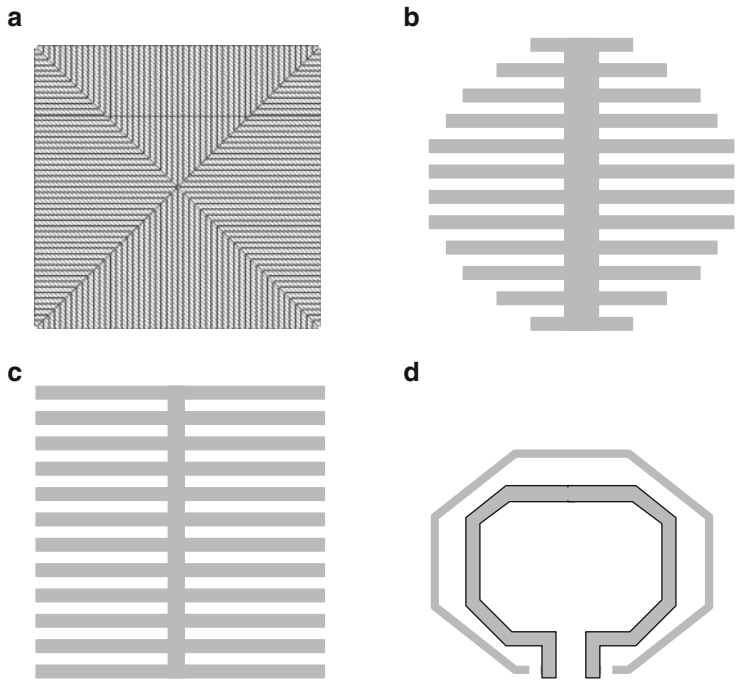

Fig. 3.6 Different ground shields: patterned (**a**), fish-bone (**b**), array (**c**), and open ground ring around inductor (**d**) [41, 118]

3.1.4 Cross Talk Shielding and Grounding

The small dimensions of mm-wave circuits together with the requirement of short interconnects can potentially lead to electromagnetic coupling and cross-talk between different parts of the circuit. Noise injection through different sources, if not controlled, can easily couple to circuits such as oscillators and, up-converted, deteriorate the spectrum purity. On the other hand, a variation in ground potential, which is the lower reference for signal voltages over the chip, can give rise to erroneous voltage levels and common-mode variations in circuits. These undesired characteristics can be controlled or minimized to varying degrees by application of various RF grounding and isolation techniques.

The main aim of grounding and shielding is either to isolate the components from each other or to surround them with ground planes and guard-rings which can act as a sink for interference generated by these circuits. A few of these techniques which have been widely employed in this work during layout of synthesizer and components are explained below:

- Utilizing the multiple layers available in modern CMOS processes, sensitive RF traces can be encapsulated in a cage like structure, sometimes referred to as a Faraday Cage This is shown in Fig. 3.7 where dimensions have been exaggerated for illustration. In this structure, the top and bottom layer of the metal stack are grounded and act as a termination for electric field lines. These metals are connected with a large number of vias on either side of the signal trace to form a cage-like shield.
- For short interconnects, if the circuit or signal periphery does not allow the above isolation technique, the coupling and cross-talk between adjacent circuits or interconnects can be reduced by placing a ground plane in close proximity as shown in Fig. 3.8.
- Long interconnects for transporting RF signals from the bond-pads to the circuit and vice versa are unavoidable. Utilizing normal metal traces for this purpose introduces impedance mismatch, resistive losses, delay and coupling with other parts of the circuit. Transmission lines (Tlines) offer a useful solution for this problem by providing an impedance matched environment for the signal and minimizing the cross-talk.

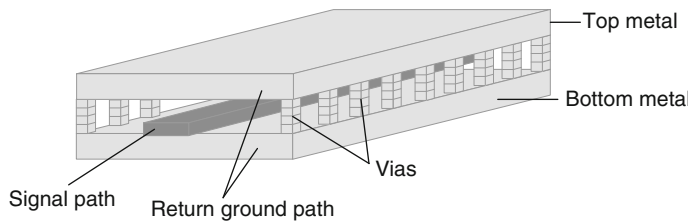

Fig. 3.7 Sensitive signal trace encapsulated in a Faraday Cage like structure for isolation

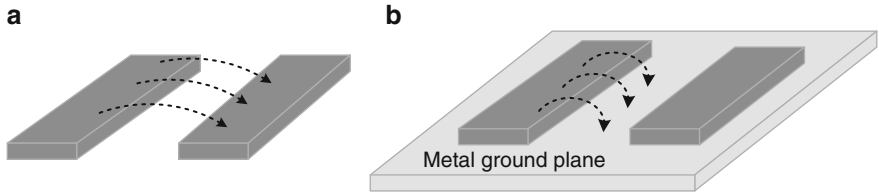

Fig. 3.8 Coupling (cross-talk) between two adjacent metal traces (**a**), and metal traces with a ground plane acting as termination to reduce coupling (**b**)

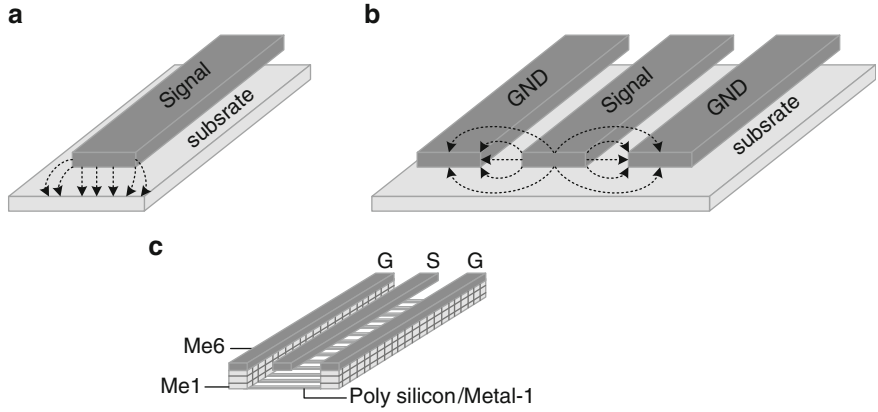

Fig. 3.9 Transmission lines: micro-strip (**a**), coplanar waveguide (**b**), and coplanar used in this work (poly-silicon lines are very finely spaced and are shown exaggerated here) (**c**)

Two main types of transmission lines are micro-strip and coplanar waveguide as shown in Fig. 3.9a and b. For the micro-strip line, field lines are terminated in the lossy substrate. To avoid the loss, a layer of metal can be used between the signal line and substrate. However, because the ground is now closer, the lines must be narrower to maintain the same impedance. Consequently, such transmission lines may not be adequate in applications where large current needs to be delivered. The other transmission line is the coplanar waveguide that has grounds besides the signal line on both sides. As the ground is at the same height as the signal-carrying conductor, ideally a large fraction of the field lines is terminated in the metal at the same height. As a result, there is less penetration of field lines into the substrate and hence lower loss. Another advantage is the provision of an additional degree of freedom as now both signal line width and separation from ground line can be adjusted. This makes it possible to achieve the desired impedance while using wider lines. The down side of coplanar transmission line is the required silicon area for ground conductors on both sides. However, this is not an issue, as mm-wave circuits are usually bond-pad limited with vacant area around the core circuits.

In this work, coplanar waveguide based Tlines are invariably used for long interconnects from the bond-pads and vice-versa. The ground plane is a "wall" like structure around the signal line and consists of all metal layers connected through a

large number of vias. A patterned polysilicon or metal-1 is placed underneath the signal path to further reduce the fields reaching the low resistive substrate.

- The importance of a ground plane for shielding as well for a stable reference voltage is evident from the above discussion. It is also important that all localized ground planes are connected to each other to provide an identical ground reference for every signal in the circuit.

To address this issue, in this work, a symmetric ground block is proposed which consists of all metal layers (Me1–Me6) and is also connected to substrate via substrate contacts. The construction of a single block is carried in a way so that an array can easily be generated to yield a meshed ground plane. The steps in the construction are depicted in Fig. 3.10.

The ground connection is not only important for signals travelling in an integrated circuit but also critical for the measurement probes used for on-wafer measurements. Usually, three to four probes, for instance single-ended (ground-signal-ground or GSG), differential (ground-signal-ground-signal-ground or GSGSG) and DC probes surround the IC. The electrical connection of all ground bond-pads ensures the same lower reference voltage for signals. In this work, the ground pins of orthogonal probes are connected by an L-shaped metallization corner whereas the ground pins within the same probe are also connected using a lower metallization layer below the signal pads. This is illustrated in Fig. 3.11.

- Modern CMOS processes have strict design rules for layout of integrated circuits, one of which is the specified density of metals over the complete chip. For low frequency circuits this requirement can be fulfilled by automatic tiling procedures during which metal "tiles" are placed all over the chip to fulfill density requirements for each metal layer. This approach can be hazardous for mm-wave circuit layouts due to the resulting coupling.

In this work, the above mentioned ground meshing is extensively utilized in the un-used chip areas to fulfill the density requirements as it includes all metal layers and contacts. Furthermore, the automatic tiling is blocked for sensitive RF paths and components and dummy metals are placed manually to avoid coupling and performance degradation.

- The small dimensions of mm-wave ICs imply that the measurement probes are in close proximity to each other resulting in cross-talk. We define two types of cross-talk. First, inter-probe cross-talk due to capacitive or radiative coupling between two different probes and second intra-probe coupling due to mutual coupling between signal lines of the same probe. In addition to shielding and grounding techniques explained above, the inter-probe cross-talk is reduced by placing them sufficiently apart as suggested in their specifications. Furthermore, the grounding used around the pads minimizes the radiation to other probes. The intra-probe cross-talk is minimized by always utilizing probes having a ground pin between two signal pins. The GSGSG probe offers much less cross-talk as compared to a GSSG probe as shown in Table 3.1 [29].

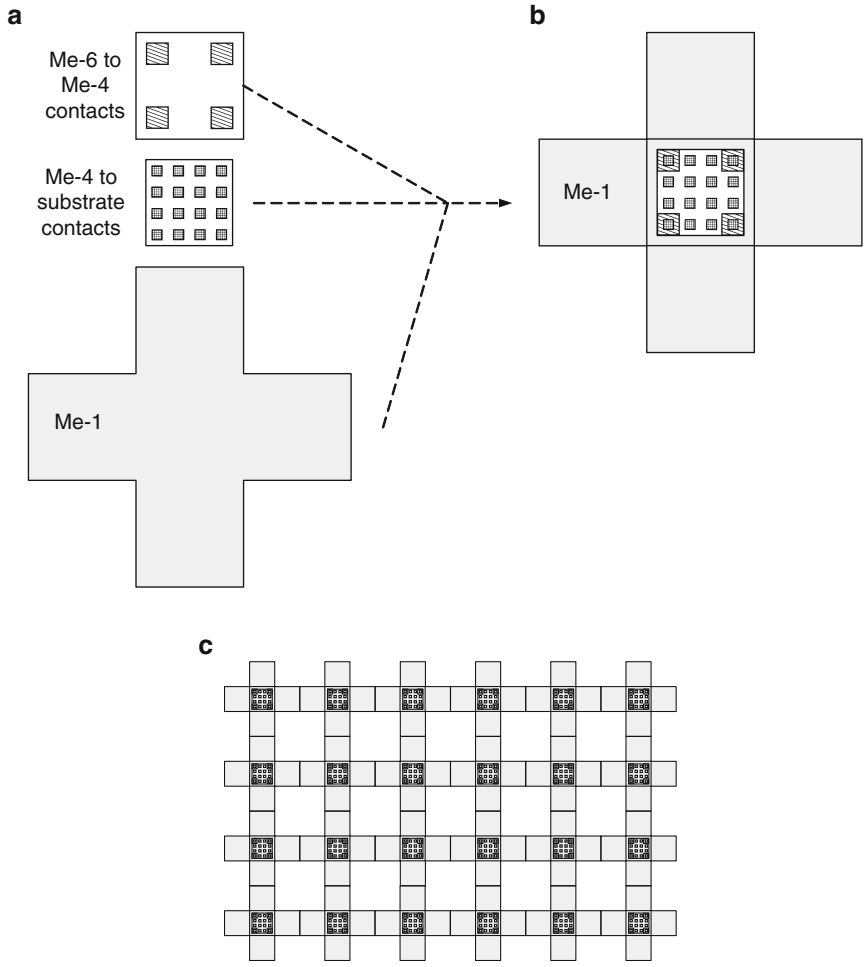

Fig. 3.10 Construction of meshed ground; metals and contacts (**a**), basic ground block (**b**), and a meshed ground plane (**c**)

- DC power supplies also contribute noise in an integrated circuit and can cause supply "bounce" due to voltage transitions and the associated current variation from the supply (dI/dt). As a synthesizer consists of purely analog circuits such as a VCO as well as digital components such as a PFD, using a common supply voltage for digital and analog can deteriorate the phase noise performance of the synthesizer. Therefore, in this work, on a layout level this problem is addressed by defining separate power supply domains for analog and digital components which are isolated from each other using the techniques mentioned earlier. Furthermore, this problem is also tackled on a circuit level and will be explained in subsequent chapters.

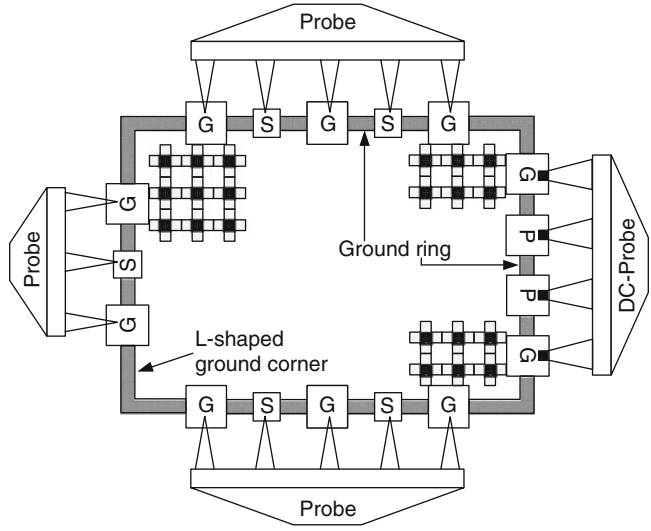

Fig. 3.11 All ground pads connected via metallization layers

Table 3.1 Cross-talk comparison between GSGSG and GSSG probes [29]

Probe structure	Cross-talk (%)	Termination structure
GSGSG	1.0	Open
GSSG	4.0	Open
GSGSG	0.3	50 Ω
GSSG	3.5	50 Ω
GSGSG	2	Short
GSSG	14	Short

3.2 Measurement Setups

At low frequencies, as a matter of tradition, an under-par performance of a circuit is usually attributed to inaccuracies of device models, analysis or circuit design flaws. However, at mm-wave frequencies it is very much plausible that the method or equipment used for measuring the circuits is responsible for false results. Therefore, the second non-circuit design challenge at mm-wave frequencies is the reliable measurement of circuits.

Integrated circuits can be measured either by enclosing them in a package and using bond-wires to connect them to the outside world or by on-wafer probing. As IC's have to be finally marketed in packaged chips, the associated packaging technologies and techniques require extensive study. However, it is not discussed in this book as all circuits have been measured by on-wafer probing. This method,

although providing a quick way of measuring and characterizing circuits, leads to a variety of challenges particularly at mm-wave frequencies and will be discussed in this section.

3.2.1 Dedicated Instrumentation

The first obvious requirement for on-wafer measurements is the set of equipment necessary for a particular measurement. At mm-wave frequencies, this points to setting-up a complete pool of dedicated and specialized equipment, cables, connectors, probes, adapters, waveguides and other such material. In addition to being costly, these require careful and precise usage to achieve successful measurements. A few considerations are enlisted below:

- Although there has been development towards high frequency measurement equipment such as vector network analyzers (VNAs), spectrum analyzers (SAs) and signal generators (SGs) in the last decade, they are still in the "catching-up" phase as compared to the rapid development of integrated circuits towards the mm-wave regime. Consequently, indirect measurement methods have to be adopted, resulting in uncertainty and inaccuracies.

As an example, consider a measurement of an oscillator operating in the V-band (50–75 GHz). As there is no single-box PSA available operating above 50 GHz, external mixers have to be employed to extend the frequency range to the desired band. A typical measurement setup is shown in Fig. 3.12. These harmonic mixers exhibit frequency dependent loss which is difficult to calibrate. The result is an increase in the noise floor of the spectrum analyzer as well as un-calibrated output power levels. Consequently, phase noise of the oscillator becomes increasingly difficult to measure.

An alternative of the above setup is designing an on-chip mixer and down-convert the oscillator frequency to within the range of the spectrum analyzer and thereby extract its performance indirectly. In such a scenario, the mixer needs to be characterized separately so that its affect on a VCO measurement can be subtracted. Extra chip area and design time are two major drawbacks of this approach.

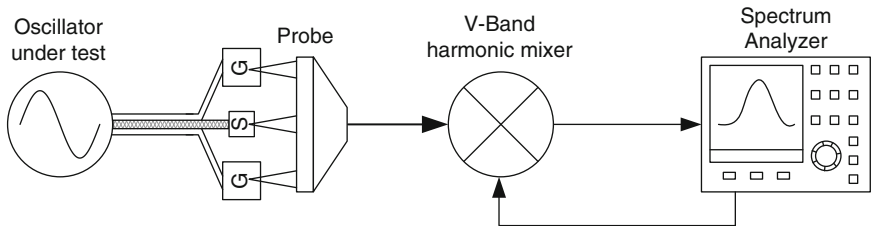

Fig. 3.12 Indirect measurement of a V-band oscillator

- Another important component for on-wafer measurements are high frequency probes. The fundamental role of the probes is to transition the RF signal from one transmission medium to another. For instance, the measurement cables may be coaxial while the wafer has micro-strip or coplanar waveguide based transmission lines carrying the RF sign-als. The selection of the probe, based on operating frequency range and layout of the chip is an important factor as incorrect probes can introduce losses degrading the overall measurements.

The probe position and alignment (in z-direction) on the bond-pads is critical for correct mm-wave measurements especially during calibration and de-embedding procedures (explained in next section). Two such scenarios are shown below. In Fig. 3.13a, the probe-tips are not in-line in y-direction giving rise to mismatch in the measured differential output. In Fig. 3.13b, the probe-tips are not aligned in the z-direction, due to which one of the differential outputs does not have reliable contact to the bond-pad. This allows common-mode noise to pass and corrupt the measured output.

- Only cables, connectors and adapters suitable for mm-wave frequencies should be used in measurements. Smaller wavelengths demand smaller dimensions of the cables and connectors in order to circumvent excitation of circular propagation modes. For mm-wave measurements, this means that common SMA and 3.5 mm accessories should not be used. Although the smaller 2.92 mm is mate-able with SMA, for best performance and precision, a uniform environment using the same precision 2.4 or 1.85 mm connecters should be utilized.

Signal connections, no matter how carefully made, are not perfect at mm-wave frequencies. The small dimensions contribute to signal loss which typically rises with frequency. In case of coaxial cables, impedance and insertion loss varies with different cable routing. Furthermore, bending and stretching cables changes their dimensions, and thus affects signal propagation. This is particularly critical when measuring phase sensitive circuits (I-Q VCOs, phase shifters etc) where matching is of utmost importance.

To address the above mentioned source of inaccuracies, semi-rigid cables and solid waveguides are employed in this work to minimize connection variations during measurements and enable accurate measurements. A measurement picture showing these components is shown in Fig. 3.14.

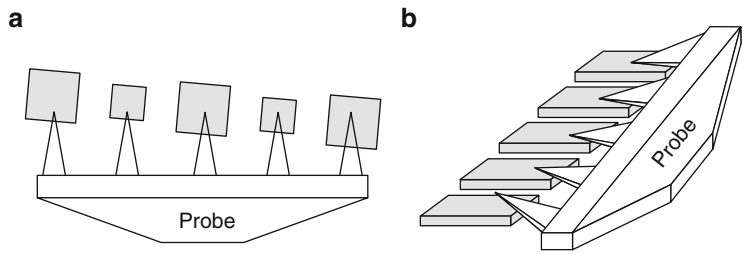

Fig. 3.13 Probe positioning error in y-direction (**a**), and error in z-direction (**b**)

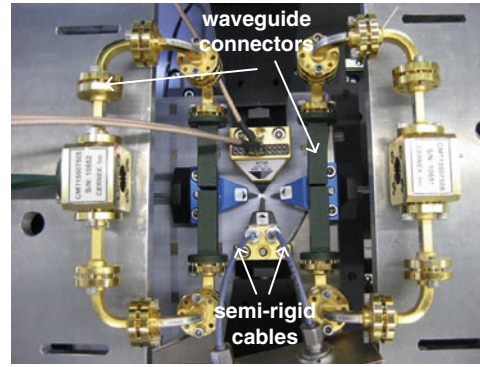

Fig. 3.14 Measurement setup with wave-guide connectors and semi-rigid cables

3.2.2 Calibration and De-embedding

The preceding discussion illustrates that on-wafer measurement of integrated circuits involves a variety of external equipment, cables, connectors, adapters, terminations, etc. As a result, the measurements observed on a VNA or SA include the effects and non-idealities of the above. The solution of this is to move the measurement plane (or reference plane) from inside the equipment to the real device-under-test (DUT). This is accomplished by two processes namely calibration and de-embedding by which the undesired contributions in the measurements are "backed-out" or "subtracted" from the overall measurement. This is illustrated in Fig. 3.15.

The first procedure by which the measurement plane is shifted from the equipment to the probe-tip is called calibration. In this process, prior to measuring the DUT, commercial impedance standard substrates (ISS) are used to account for imperfections of VNA, cables, connectors and probes. The known calibration standards like open, short, load, through and line (present on the ISS) generally have no special relationship to the device under test except that both must accommodate the probes spatially. Achieving effective calibration for accurate measurements at mm-wave frequencies is a significant challenge and some considerations employed in this work are discussed below:

- The calibration standards on a particular ISS need to be accurately defined in a VNA correction algorithm. Inaccurate calibration standards result in corrected measurements that contain residual errors. It is to be noted, that the specific electrical behavior of the standards depends upon the probe pitch (distance between two adjacent probe tips). Therefore, the calibration data for a particular ISS is specified only for a specific probe spacing and ISS combination. The probe type, for instance GSG or GSGSG also need unique calibration data and ISS for the latter should not be used for the former to maintain calibration accuracy.

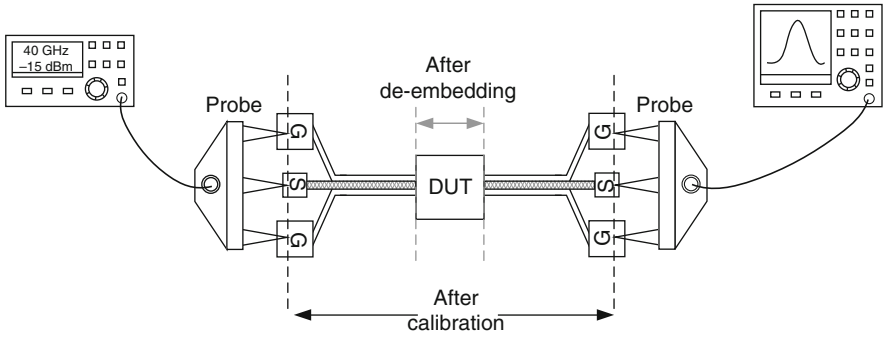

Fig. 3.15 Illustration of calibration and de-embedding procedures for accurate measurements

- The importance of the probe position on the bond-pads (as mentioned in the previous section) is more evident during a calibration procedure for mm-wave measurements. It is observed that the percentage of error crosses the acceptable range if two opposite probes do not land at the same location on a calibration standard (in a two port measurement). A common mistake is to readjust the probes when moving from one calibration standard or DUT to the other. Before beginning calibration, the probes should be set once and their position should not be changed once calibration has started. Movement of the probes will change the standard's parasitics, in particular its inductance and can potentially cause calibration failure [30].
- Another key issue is the calibration validity with time. It is experienced that the percentage of tolerable error increases significantly for mm-wave frequencies after a few minutes have elapsed after the first calibration. An example of this is shown in Fig. 3.16 where the blue samples correspond to the original calibration result and the green samples refer to the calibration validity checked after approx. 7 min have elapsed. The latter shows that the percentage variation in s-parameters is above the acceptable level especially beyond 40 GHz. The slight jump at 40 GHz is attributed to the non-ideal behaviour of a differential to single-ended hybrid which has an upper frequency range of 40 GHz.
- The wear and tear of the ISS due to repetitive contact degrades the calibration quality and using damaged samples does not provide acceptable error percentages in most cases. This affect is particularly visible at frequencies above 40 GHz.
- User interaction with the measurement setup needs special attention. Even a minor bend or kink in a measurement cable due to a physical contact or vibration can introduce impedance mismatch at mm-wave frequencies and potentially render the calibration invalid.

The small dimensions of mm-wave circuits and components as compared to the total bond-pad dimensions necessitate the need of transmission lines which can transfer the signal from the DUT in an impedance matched environment to the probe-tips. However, this means that contribution of the pads and the T-lines also need to be subtracted from the overall measurement results. This process by which

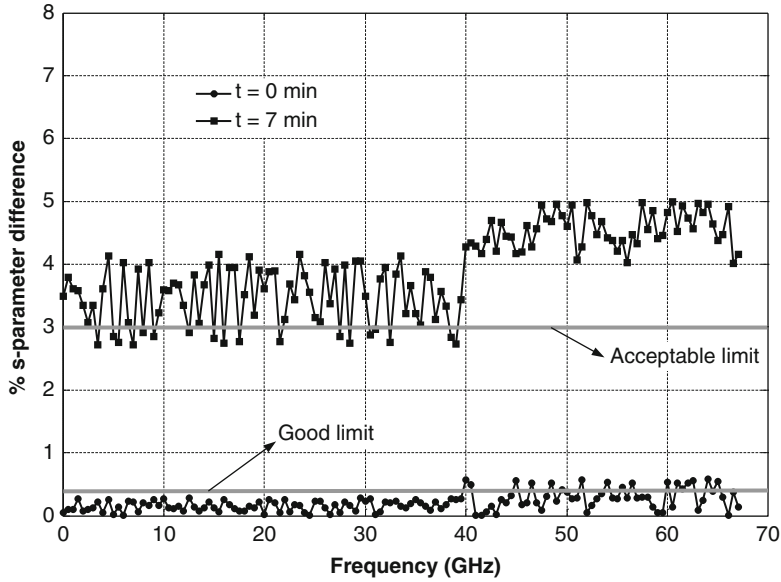

Fig. 3.16 Calibration accuracy variation with time

the measurement plane is shifted from the probe-tips to the DUT location is termed as de-embedding.

The bond-pads and interconnect lines can be de-embedded if they can be characterized through known de-embedding structures and their associated models. The simplest technique to de-embed the DUT is to fabricate identical test structures on the wafer and not include the DUT. For accurate de-embedding at mm-wave frequencies, an open, short and load structure is required as depicted in Fig. 3.17. The s-parameters of these structures are measured after calibrating the system and post processing is carried out analytically to de-embed the undesired contributions from the overall measurements. A practical example will be presented in Chapter 4.

To improve accuracy, measurements carried out in this work take into account the abovementioned improvements during calibration and de-embedding. Well defined and accurate ISSs are utilized and placed on an auxiliary-chuck space so measurement of the DUT can be carried out immediately after calibration within the time-span of calibration validity. The measurement setup is fixed for measurements and re-calibration is done in case of physical movement of cables etc.

3.2.3 Stability and Repeatability

Repeatability is measure of similarity between measurements under identical conditions with the same measurement equipment including cables, connectors etc. It is

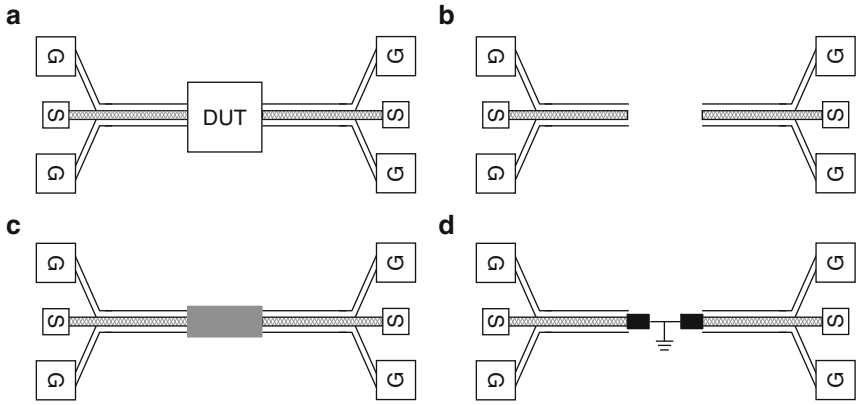

Fig. 3.17 De-embedding structures: with DUT (**a**), open (**b**), short (**c**), and load (**d**)

also a function of inherent stability of individual components being used in the measurement system. The sensitivity of mm-wave measurements due to factors mentioned in the preceding sections gives rise to variations in the measured results.

Variations between successive measurements can be reduced by following a careful approach during measurements. Some of these, adopted in this work are mentioned below:

- The measurement environment should be kept quiet after setting-up the measurement system. Sources of noise should not be placed in close proximity of the probe station. In an oscillator measurement, the noise from these external sources can be picked up by the probes as common-mode, and up-converted close to the carrier frequency. This affect is particularly visible during phase noise measurements of oscillators which demonstrate variations of 1–3 dB between successive measurements. The microscope lighting should also be turned-off after probes are positioned on the wafer to reduce temperature variations.
- A probe contact with all pins equally pressed on the bond-pads is required to ensure proper signal transition and ground contact. The over-travel[2] specifications of the probe tips on the pads should be adhered to.
- Modification in the length or bends of the cabling is another source of variation between mm-wave measurements. Therefore, physical contact with the system should be avoided and the measurement system should be identical for all measurements.
- In order to average out deviations due to measurement variations a number of die-samples should be measured. This yields statistical information related to measurement repeatability on the same die as well as for die-to-die variations.

[2]The distance travelled by the probe-tip after touching the bond-pad to achieve firm contact.

3.3 Conclusions

At mm-wave frequencies, the effect of layout parasitics and sensitivity of measurements requires special attention. This chapter summarized the techniques employed in this work to address the non-idealities of layout and measurements. For mm-wave layout there are "no-rules" but only guidelines. As the circuit dimensions approach the wavelength of signals on-chip, distributed effects begin to dominate and lumped element analyses are no longer valid. Furthermore, the passive values required for different circuits are of the same order as parasitics of transistors and interconnects. Due to the above reasons, un-accounted RF interconnects as small as $\sim$10 μm can cause drift and unreliable measured results. Therefore, designers need to identify the minimum tolerable interconnect length based on the frequency and the circuit application. The floor-planning of passive and active components should be done in a way to minimize interconnect lengths. In addition, using circuit editors for RC-extraction and EM-solvers for inductance extraction for critical interconnects can provide a reasonable match between simulations and measurements. In order to avoid substrate losses, cross-talk and coupling between components, shielding techniques such as meshed grounding, coplanar transmission lines, and guard-rings should be utilized.

The measurement set-ups for mm-wave circuits are sensitive to losses, mismatch and variation in the equipment, cables, connectors, probe position and temperature. Therefore, accurate and regular calibrations need to be carried out to keep the measurement plane as close to the DUT as possible. Furthermore, the measurement setup should be fixed and no physical change in cabling should be allowed to ensure repeatable results. The noise of the measurement equipment should be minimized by proper grounding as it could be picked up by the probes if they are not enclosed in a chamber. Ambient as well as temperature close to DUT should remain relatively constant to avoid temperature dependent variations in the results. A considerable number of samples should be measured and results averaged to reduce contributions of these non-idealities in the measured results.

Chapter 4
Design of High Frequency Components

Abstract The design and implementation of the PLL front-end components, including the voltage controlled oscillator and the prescaler is presented in this chapter. The prescaler circuits include static and injection locked frequency dividers at 40 GHz and only the latter type for 60 GHz. A dual-mode ILFD is also presented to combine the functionality of divide-by-2 and divide-by-3 operation. The voltage controlled oscillators are also designed for 40 and 60 GHz operation frequencies. The 60 GHz circuits include an actively coupled and a transformer coupled version for quadrature signal generation. The last part of the chapter presents the combined front-end circuits.

Keywords Voltage controlled oscillator · Injection locked frequency divider · Static frequency divider · Current mode logic · Transformer coupling · Varactor · Multi-mode operation

Frequency synthesizer components operate at varying frequencies. The voltage controlled oscillator and the first frequency divider stage, together termed as synthesizer front-end, work at the highest frequency and therefore are the most challenging components. Prior to complete synthesizer integration, a step-wise approach is adopted, first to design the individual components of the front-end and second to integrate them. This assists in understanding the challenges of each component and the interaction between them.

This chapter focuses on the synthesizer front-end integration as well as individual component design as highlighted in Fig. 4.1. Section 4.1 begins with an overview and comparison of different prescaler architectures suitable for mm-wave operation. Characteristics such as locking range (LR), power consumption, quadrature generation and phase noise are considered as comparison metrics. Theoretical analysis of static frequency divider (SFD) and injection locked frequency divider (ILFD) is presented next. The ILFD analyses in published literature are usually based on small signal operation, whereas ILFDs actually experience large signal swings; therefore a discrepancy is present in

H.M. Cheema et al., *60-GHz CMOS Phase-Locked Loops*,
DOI 10.1007/978-90-481-9280-9_4,

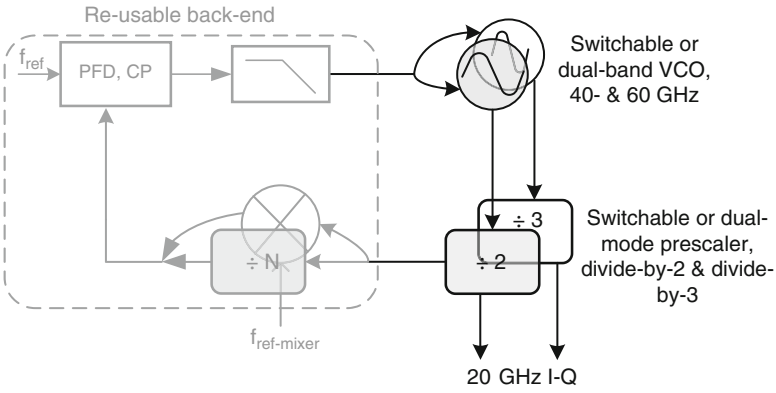

Fig. 4.1 Highlighted synthesizer front-end components

the calculated and simulated (or measured) locking range which has to be kept in mind.

Sections 4.1.2–4.1.6 present four integrated prescaler circuits for the proposed synthesizer. The first is a static divider based on D-latches which are optimized for high frequency and broadband operation. Next are two injection locked frequency dividers targeting the 40 and 60 GHz bands and include techniques to enhance injection efficiency thereby increasing locking range. The 40 GHz ILFD is designed to provide quadrature (I-Q) 20 GHz outputs as required by a project partner. As the proposed synthesizer aims to provide LO signals for sliding-IF as well as direct conversion receivers, a dual-band prescaler can alleviate the requirement of two separate (or switchable) dividers. To fulfill this requirement, Section 4.1.6 presents a new dual-mode ILFD which can divide by 2 or 3 based on the input injection frequency. A monolithic transformer which is utilized in the above dual-band ILFD as well as in a later VCO circuit is presented in Section 4.1.5.

The other key high frequency component in a synthesizer is the voltage controlled oscillator. Section 4.2, starting with a comparison of conventional VCO architectures, reviews the theoretical analysis related to oscillation conditions, tuning range and phase noise. The 60 GHz frequency band poses stern tuning range (TR) requirements for VCOs as more than 10% TR is required to cover the complete un-licensed spectrum. Furthermore, varactors, which are invariably used as tuning elements for altering VCO frequency, have low quality factors at these frequencies and become the dominating factor as compared to inductors. Section 4.2.3 presents a number of varactor tuning arrangements aiming to improve their quality factor and providing the required tuning range at the same time. One of these is utilized in a 40 GHz VCO presented in the same section. Synthesizers for direct-conversion receivers require 60 GHz quadrature LO signals. Therefore, the next two sections are dedicated to two approaches; the first is based on actively coupling two identical 60 GHz VCOs by using extra transistors whereas the second

is based on transformer coupling between the I and Q VCOs. The transformer presented in Section 4.1.5 is reused in the latter design. In the same line as the prescaler, a flexible synthesizer requires a switchable or dual-band VCO able to operate at 40- and 60 GHz. Section 4.2.6 presents a number of design approaches and associated challenges to achieve this task.

The next step, after implementation and measurement of VCO and prescaler separately, is integration of the two components to form the synthesizer front-end. As the VCOs and ILFDs are based on LC tanks, their frequency selectivity makes the integration a considerable task. The tuning range of the VCO and locking range of the ILFD should coincide with each other for correct operation. A shift in any of them due to design inaccuracy or layout parasitics can result in failure for meeting the target specifications. Section 4.3 presents synthesizer front-ends for 40 GHz as well as 60 GHz based on the corresponding VCO and prescaler circuits.

4.1 Prescaler

A prescaler is the first frequency divider stage in the synthesizer feedback loop. For low frequency synthesizers the prescaler does not necessarily need to be treated separately as the requirement specifications are not stringent and thus the design is straightforward. On the other hand, for mm-wave or 60 GHz synthesizers the prescaler needs to operate at the highest frequency of the loop. Furthermore, for FC techniques based on a two-step down conversion (Section 2.2) and using the prescaler outputs for a second mixer, the specifications become even more demanding.

The selection of a prescaler architecture for 60 GHz synthesizers needs careful consideration. Firstly, it should be able to cover the complete VCO tuning range along with some margin for PVT variations as well as for a shift between simulations and measurements. For a direct conversion architecture this implies a 7 GHz operation range which is challenging to achieve. Secondly, the prescaler should be highly sensitive, as owing to power consumption constraints and interconnect losses, the VCO output power can be quite low and can vary over the tuning range. Therefore, reliable frequency division for all VCO power levels is required. Thirdly, for a two-step down conversion (or sliding-IF), prescalers need to provide accurate quadrature outputs, as IF-LO, for error free baseband data. The above requirements, in some cases, are contradicting. For instance one prescaler architecture might be able to provide inherent quadrature outputs but unable to operate at mm-wave frequencies whereas another one might operate at high frequencies but offer a narrow locking range. Therefore, architecture selection and design trade-offs have to be adopted keeping in view the most important performance specification. The next section provides an overview of mm-wave prescaler architectures which can provide division ratios of two and three as required in the proposed synthesizer.

4.1.1 Overview and Comparison of Prescaler Architectures

Prescalers for mm-wave frequencies can be categorized into digital, analog or their combination (hybrid) as shown in Fig. 4.2. The digital class of dividers is sub-divided into static and dynamic FDs whereas the analog consist of regenerative or miller divider and injection locked frequency divider. Travelling wave FD, a hybrid of digital and analog presented in [31] for low frequencies is analyzed in this book for mm-wave operation.

In order to compare the performance metrics of the above dividers, their operating principles are discussed next.

- Static frequency dividers (SFDs) are one of the most widely used class of dividers [32–38]. They are usually based on an edge-triggered flip-flop in a negative feedback loop. The flip-flop is composed of two master and slave D-latches which are driven by anti-phase clock pulses. Figure 4.3 shows a standard SFD along with the associated timing diagram. The dividing operation is achieved by connecting the inverted slave outputs to master D-latch inputs. Seen as a two stage ring oscillator, static frequency dividers can provide highly matched quadrature outputs which are required in the two step down-conversion in a transceiver.

In principle, any type of latch can be utilized in a SFD. However, traditional CMOS rail-to-rail implementations lead to long rise and fall times, resulting in low operation frequencies. In addition, the single-ended structure also suffers from supply noise coupling, potentially introducing jitter in the output. MOS current mode logic (MCML or just CML) sometimes also referred to as source coupled logic (SCL), is a better alternative for D-latch implementation [39, 40]. This logic family is characterized by, firstly, small voltage swings thus reducing the rise and fall times and enhancing the operation frequency. Secondly, the differential and current steering nature of MCML reduces the switching and supply noise resulting in a spur-free synthesizer output spectrum and lastly, it consumes a constant current, hence the name static frequency divider. A D-latch based on MCML logic is shown in Fig. 4.4.

The maximum operation frequency of the SFD depends on the propagation delay from input D to output Q in a D-latch and can be estimated by

$$f_{\max} \leq \frac{1}{2\tau_{pd}} \tag{4.1}$$

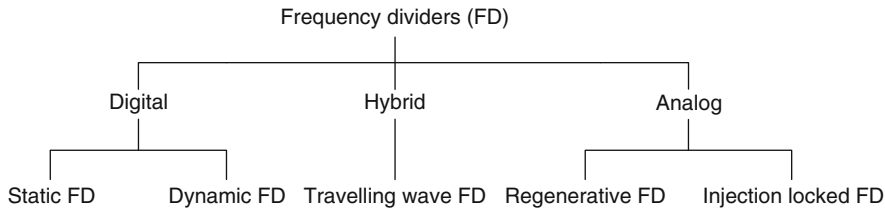

Fig. 4.2 Prescaler categorization

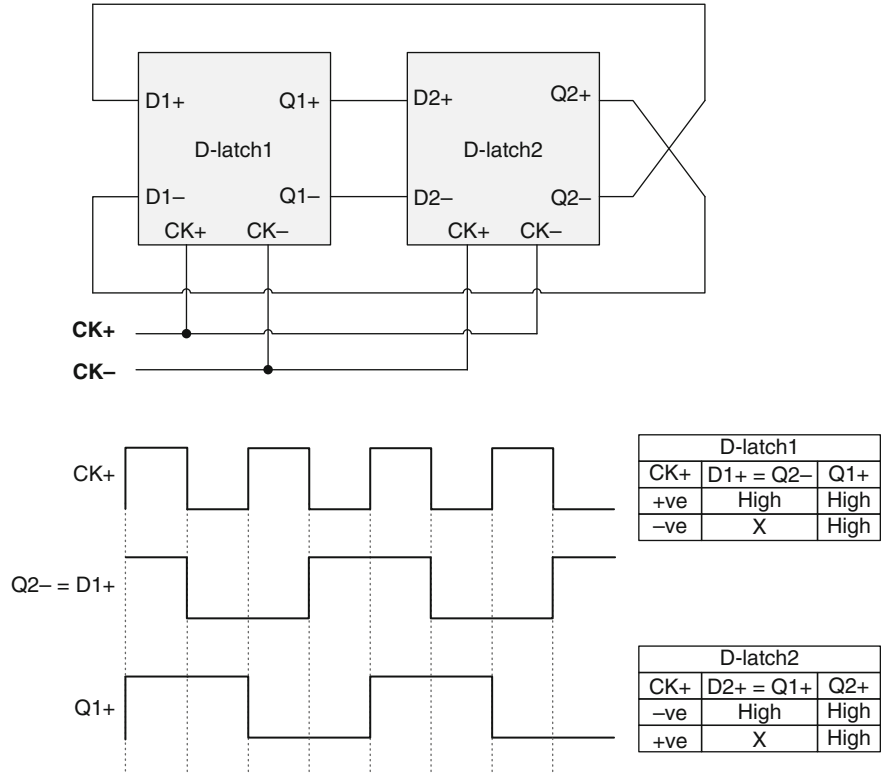

Fig. 4.3 Static frequency divider

where τ_{pd} is the propagation delay. In a differential circuit (such as CML logic) τ_{pd} for rising and falling edge is identical and in first order, proportional to the charging time constant τ_L, i.e.,

$$\tau_{pd} \propto \tau_L = R_L C_L \tag{4.2}$$

where R_L is the load resistance and C_L is the total capacitance at the output node consisting of parasitic contribution from the latch transistors M3–M4, output buffer transistors (not shown in Fig. 4.4) and layout interconnect. It is evident that, to maximize speed, τ_L or R_L and C_L should be minimized. However, there is a trade-off present between the two passive values. If R_L decreases, the gain $g_m R_L$ of the transistors M1–M2 also decreases. In order to compensate this decrease, larger transistors are required to boost the g_m thus increasing the total capacitance. On the other hand if C_L is reduced by using smaller transistors, R_L needs to be increased to maintain a sufficient output voltage swing. Techniques such as inductive peaking [32, 33], distributed loading [36] and LC-tank loading [34] have been employed to increase the bandwidth of SFDs. The SFD

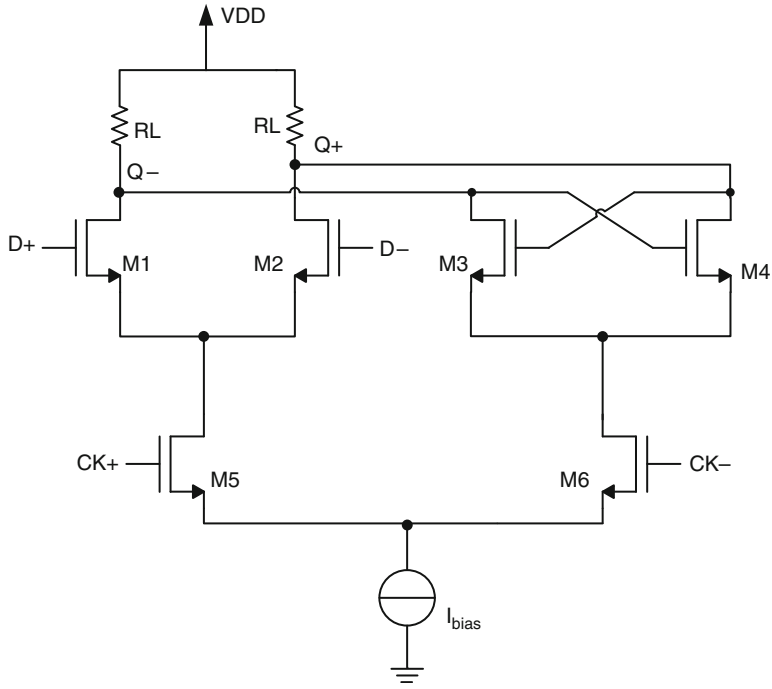

Fig. 4.4 A standard MCML D-latch

presented in Section 4.1.2 utilizes the inductive peaking to enhance the operation frequency.

Theoretically, SFDs can operate up til very low frequencies; however, if a sinusoidal input is used (as in practice from a VCO), they might not work below a certain frequency due to low slew rate. This is because the slow transition of CK+ and CK- can turn-on both latches simultaneously, making the loop transparent for a short duration. As a result, false switching at the output is seen due to the "racing" phenomenon [41]. Fortunately, in a prescaler design the lower frequency limit of the SFD is of less concern as it is connected directly to the VCO which is operating at the highest frequency of the synthesizer.

A large number of static frequency dividers have been reported in the frequency range uptil 40 GHz [32, 33, 35–37, 42, 43] and a few implementations above 60 GHz using SOI technologies have also been demonstrated [44–47].

- The second sub-category of digital dividers is the dynamic FDs. These distinguish themselves from the static counter parts in the implementation of the D-latches used in the flip-flop and the current consumption which only occurs during a portion of a clock cycle [48–52]. Two variations of dynamic dividers are shown in Fig. 4.5.

In the first dynamic divider, when CK is high, the first latch acts as a pseudo-nMOS inverter and the input signal is clocked into the storage capacitor C_p.

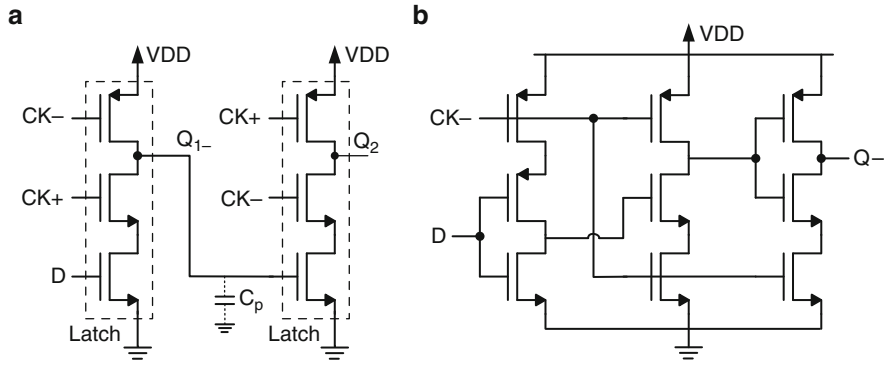

Fig. 4.5 Dynamic frequency divider: dual-clock pseudo-nMOS (**a**), and true single phase clocking (TSPC) (**b**)

When the CK goes low, the first latch becomes opaque and the second latch is switched ON, transferring the signal to the output node. The unavailability of complementary outputs is a drawback of this design as it cannot be connected to subsequent divider stages which require complementary signals as their inputs. A solution to the latter problem is the dynamic divider in Fig. 4.5b which is driven by a single phase clock. This type of dynamic divider is called true single phase clocking (TSPC) divider. The operation of this divider consists of a pre-charge phase and an evaluation phase. When the CK is low, the output is pre-charged to VDD through the PMOS devices. During this phase the divider does not consume any current as the lower part is OFF. When the CK is high, the evaluation period starts and output stays high or goes low based on the implemented input logic.

The advantage of dynamic dividers over SFDs is reduced power consumption and less number of transistors. However, for mm-wave prescaler design, drawbacks of dynamic dividers are more dominant. Firstly, unavailability of inherent complementary and quadrature outputs is a major disadvantage. Secondly, common-mode noise is visible at the output due to the single-ended topology and is more sensitive to parasitic effects such as leakage, charge redistribution and clock feed-through [53]. Lastly, due to limited charge retention this class of dividers is unable to reach the mm-wave regime and the highest frequency reported in a 0.1 μm SOI technology is 18 GHz [51].

- Prior to the description of the analog class of dividers, an alternative frequency divider architecture is considered which does not strictly fall in any of the two distinct classes. This is termed as travelling wave divider (TWD), and was first presented in [31] and re-used in [54]. Although both these implementations are based on bipolar technologies and operate at low frequencies around 2 GHz, in this work, feasibility of this architecture was analyzed for mm-wave frequencies in bulk CMOS 90 nm technology.

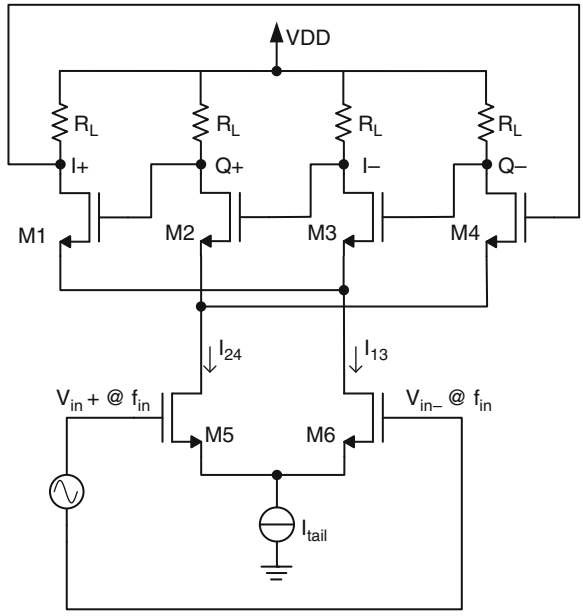

Fig. 4.6 Travelling wave frequency divider

The travelling wave divider is shown in Fig. 4.6. The circuit consists of three differential amplifiers: the input clock amplifier M5, M6 and two differential amplifiers M1, M3 and M2, M4 with complementary inputs. The drain and gate terminals of transistors M1–M4 are connected in a cyclic manner. Although the operation of this divider can be compared to two closely coupled bi-stable differential amplifiers that switch between master and slave state, the analog nature of the circuit becomes evident if current transitions between different branches of the circuit are analyzed. At the start of operation let $I_{13} = I_{tail}$ and $I_{24} = 0$ and assume that I_{13} flows only through M1 generating a drain voltage signal. As the current switches from M6 to M5 the drain signal travels (or shifts) one position to the right to the drain of M2. After four switchings of current between M5 and M6, i.e. two periods of the input clock signal the drain signal completes one cycle and hence operates as a divide-by-two frequency divider.

The travelling wave divider offers a number of advantages; firstly, the lesser number of transistors offers a simple circuit with less parasitics. Secondly, the availability of complementary as well as quadrature outputs enables its integration with a subsequent divider chain and/or a mixer for a second down-conversion step. In order to gauge the mm-wave performance of a TWD, transistor level simulations are carried out (see Appendix 1). The locking range (LR) of a frequency divider can be given as

$$LR\ (\%) = \frac{f_{\max} - f_{\min}}{f_{center}} \times 100 \tag{4.3}$$

The TWD demonstrates broadband operation with a locking range of 68% around $f_{center} = 33.5$ GHz. However, there are two down-sides of the TWD revealed by simulations. Firstly, the maximum and minimum operation frequency is susceptible to load resistance variation and secondly, the output amplitude varies over the locking range. Numerical values of these two non-ideal effects are presented in Table A1.1 and Fig. A1.1, respectively.

- The first type of the analog class of dividers is called the regenerative or Miller frequency divider (RFD), first proposed in [55]. The operating principle of the RFD can be understood by Fig. 4.7 where a mixer is placed in a feedback loop and the output is mixed with the input. The mixer generates the sum and difference components of $f_{in} + f_{out}$ and $f_{in} - f_{out}$, respectively. By placing a band-pass filter, the sum component can be filtered out and the difference component persists in the loop and satisfies the relation $f_{out} = f_{in} - f_{out}$, i.e. $f_{out} = f_{in}/2$. This configuration has a potential to work at moderate to high frequencies as it allows combined design of the mixer and band-pass filter. The latter, which in most cases is a tuned LC-tank can absorb the capacitance of the mixer and thus reach high frequency of operation.

A CMOS implementation of an RFD is shown in Fig. 4.8, where the mixer is a standard Gilbert cell and the feedback loop is formed by connecting the drains to

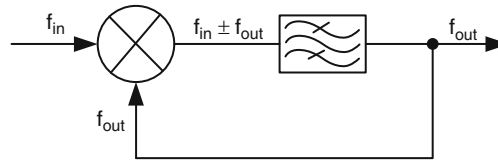

Fig. 4.7 Divide-by-2 regenerative frequency divider operating principle

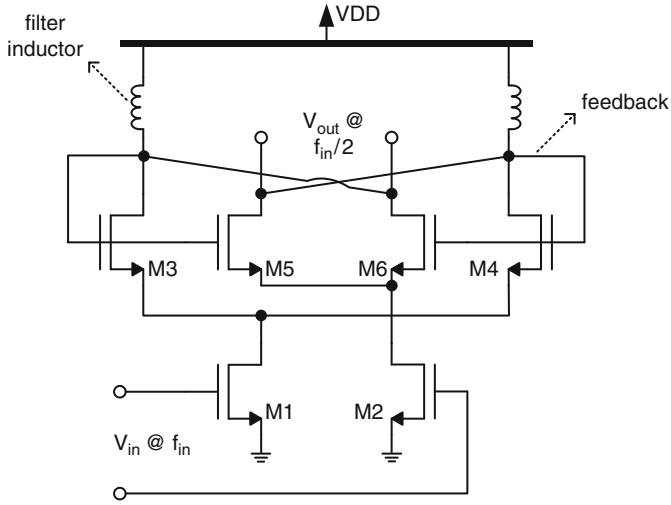

Fig. 4.8 Divide-by-2 regenerative frequency divider circuit

the gates of M4 and M3, respectively. The band-pass filter is formed by the inductor and the parasitic capacitance of the transistors. Varactors can also be incorporated to shift the pass-band frequency resulting in enhancement of operating range. Unlike the SFD, the regenerative frequency divider does not self-oscillate, i.e. if the input clock is switched OFF, the divider output will be zero as well. Due to this characteristic of the RFD, the sensitivity curves do not have local minima and are "flatter" as compared to static frequency dividers [56]. As a mixer has two input (LO and RF) ports, the output, in principle, can be fed back to any one of them resulting in two configurations of RFDs. The configuration shown in Fig. 4.8 feedbacks the signal to the LO port, whereas the other configuration returns the signal to the RF port with the input signal applied to the LO port.

A number of regenerative frequency dividers have been presented in recent years [56–58]. However, the performance for mm-wave frequencies especially at 60 GHz is not satisfactory. Firstly, the required input power is considerably higher as compared to other frequency dividers as signal loss from the RF to the LO port (or vice versa) becomes significant at these frequencies. Secondly, the locking range offered by RFDs is smaller than the digital counterparts. For instance, an improved regenerative divider at 60 GHz in [57] demonstrates a locking range of 1.8 GHz only.

- The second and promising high speed analog divider is recognized as the injection locked frequency divider (ILFD). It is based on injection locking (or pulling) phenomenon of oscillators in which it is forced to oscillate at a frequency different from its tank resonance frequency [59]. The injection locking principle can be understood as adding an external sinusoid to an oscillator as shown in Fig. 4.9. If the amplitude and frequency of the sinusoid are chosen correctly, the circuit begins to oscillate at the injection frequency f_{inj} rather than the tank frequency f_0. It is obvious that injection locking would occur only in the vicinity of f_0 where the oscillator can be pulled easily. Therefore, the locking range of such a scheme is limited to start with.

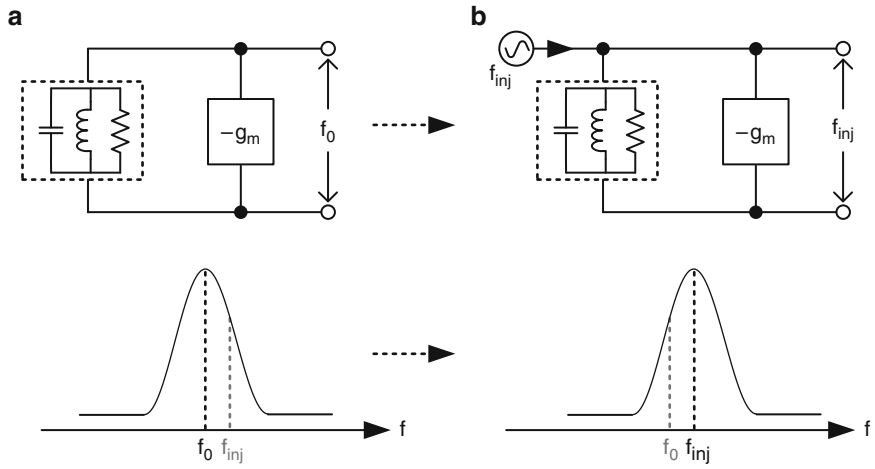

Fig. 4.9 Injection locking principle; free running oscillator (**a**), and injection locked oscillator (**b**)

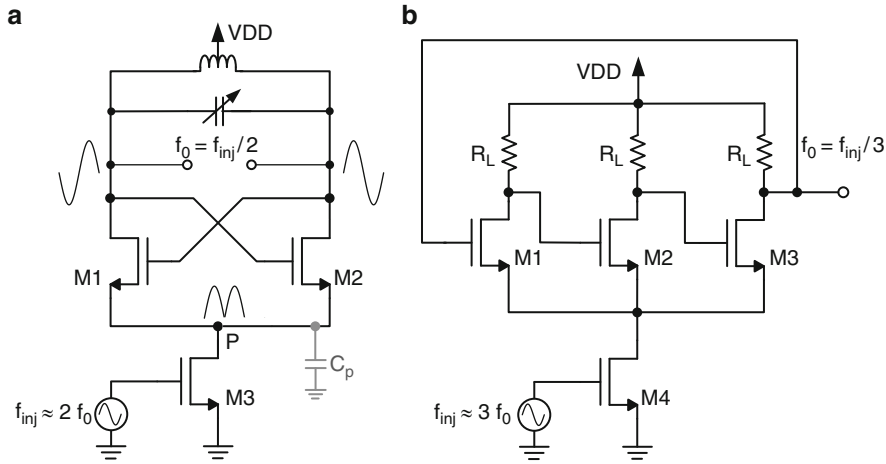

Fig. 4.10 Injection locked frequency divider; LC based divide-by-2 (**a**), and ring oscillator based divide-by-3 (**b**)

The injection locking technique can also be adopted to achieve frequency division. For instance, LC based oscillators, in addition to the fundamental component, present second harmonic of the oscillation frequency at their tail (common-mode) nodes. If a frequency approximately twice the oscillation frequency is injected at such a node, the oscillator locks to exactly half of the injected frequency. In other words, ILFD is an oscillator in which a harmonic of the oscillation frequency is locked to the fundamental frequency of the injected signal.

A simple CMOS realization of a divide-by-2 ILFD is shown in Fig. 4.10a. The core of the divider is the cross-coupled NMOS oscillator with a tank resonance frequency f_0. The signal at node P is at the second harmonic of f_0 and therefore an obvious point for external signal injection through a tail transistor M3. The injected signal mixes with the fundamental component producing a difference component which is close to the tank resonance frequency and thus locks to $f_{inj}/2$. ILFDs can also be treated as a special type of regenerative dividers, in which the non-linear active devices act as mixer, the LC tank as band-pass filter and feedback is provided by the inherent oscillator.

The injection locking technique can also be extended to implement ILFDs with higher division ratios. Divide-by-3 operation using an LC based ILFD, can be achieved by modifying the circuit in Fig. 4.10a and preserving the third harmonic of the oscillation frequency [60]. This will be explained by a practical implementation in Section 4.1.4. The same division ratio can also be achieved by injecting the signal to a 3-stage ring oscillator as shown in Fig. 4.10b [61]. Similarly, higher division ratios for instance 4, 6, 8 or even 12 are possible by using injection locking based in ring oscillators [62–65].

A number of challenges need to be addressed in ILFD designs. Firstly, due to frequency selectivity of the tank, the locking range is limited and needs to be

enhanced using circuit design techniques. The general aim of such techniques is to increase the injection efficiency by which more power of the injection signal reaches the LC tank. In the circuit of Fig. 4.10a, the parasitic capacitance at node P creates a path to ground for high frequency injection signals. This "eats-up" significant signal power, undermining the injection. To address this issue, an inductor can be added to resonate out the capacitance Cp, enlarging the locking range without extra power consumption albeit extra silicon area [66]. Another drawback of the basic ILFD circuit is the single-ended input injection, wasting 50% of injection power. An alternative topology called "direct injection" or "tank injection" can be adopted for differential injection [67]. Two examples of direct injection will be presented in Sections 4.1.3 and 4.1.6, in which the signal injection is accomplished by two switches placed across the tank still driving common-mode points of the circuits. Attaining quadrature outputs from ILFDs require extra circuits. One solution is to actively couple two identical ILFDs to generate outputs 90° spaced outputs [68]. Passive techniques such as transformer coupling or poly-phase filters can also be employed to achieve the same. The narrow locking range of ILFDs necessitates careful, design, skillful layout, as well as meticulous EM simulations especially at mm-wave frequencies. The integration of an ILFD with a VCO requires careful co-design as shift in any of them due to process and temperature (PVT) variations may destroy the locking.

An overview of frequency dividers suitable for mm-wave operation has been presented above. The choice of one topology over the other lies on the requirements of locking range, quadrature generation, power consumption, phase noise, robustness and design complexity. Table 4.1 summarizes the pros and cons of the presented architectures to facilitate design choice of prescalers for the proposed synthesizer.

Static frequency dividers while providing a large locking range consume more power and can only reach around 40 GHz using bulk CMOS technologies. Dynamic dividers are easy to design but inability to provide quadrature outputs and low operation frequency is the down-side of this architecture. Travelling wave divider offers a simple circuit implementation with quadrature outputs but it is prone to output power and locking range variations. The analog class of dividers can operate at higher frequencies as compared to the digital counterparts. The regenerative dividers offering moderate locking range are complex circuits and require higher input powers for proper division. Lastly, injection locked frequency dividers, can easily operate at mm-wave frequencies. However, to address its narrow locking

Table 4.1 Comparison of prescaler architectures

	Operation frequency	Locking range	I-Q outputs	Power	Robustness	Ease of design
Static	−	++	++	−	++	++
Dynamic	−−	+	−	+	+	+
Travelling wave	+	+	++	−	−	−
Regenerative	+	−	−	+	−	−
Injection locked	++	−−	+	+	−	−

range, circuit design solutions have to be found. The power consumption of ILFDs is the minimum among all dividers and with straightforward techniques can provide matched quadrature outputs.

4.1.2 35 GHz Static Frequency Divider

The first component design of the 40 GHz synthesizer front-end deals with the prescaler. Due to robustness and simplicity, investigation of a static frequency divider as the prescaler is carried out. The main specification to be satisfied by this component is to be able to divide the entire VCO frequency tuning range, the maximum of which is 42.3 GHz (Section 2.6). In order to achieve the above target, a number of circuit improvements are proposed which will be explained shortly. The block diagram of the divider and output buffers along with their under-lying circuits is shown in Fig. 4.11.

The SFD consists of two master slave D-latches placed in negative feedback and clocked by opposite phase clock signals. Each D-latch is based on MOS current mode logic (MCML, Section 4.1.1) and consists of two differential pairs with distinct modes of operation. Transistor pair M1 and M2 of the D-latch is termed as tracking pair (also called sensing, sampling or evaluation pair) and M3, M4 is termed as latching pair (or regenerative pair). The tail current Ibias is switched between the tracking and latching pairs by the clock transistors (M5–M7) based on the clock (CK) inputs. When the CK is high, the track pair in the first latch is active and the D inputs are transferred to outputs Q. On the other hand, when CK goes low the latch pair becomes active and the present value of Q is stored or latched. The role of the sense and latch pairs are reversed in the second latch as it is clocked oppositely to the first one. Thus, the input is transferred to the output of the divider after two clock cycles and hence the divide-by-2 operation is achieved. The outputs of both latches are buffered to achieve large output amplitude for measurement purposes.

As mentioned in Section 4.1.1, the highest speed of operation of the SFD depends on the propagation delay from input to output in a D-latch. This in turn is defined by the RC time constant at nodes Q+ and Q−, where R is the load resistance and C is the total output capacitance. The smaller this RC product, higher the frequency achieved by the SFD. In order to de-termine the load resistance, the output voltage swing of an SFD can be written as

$$\Delta V = I_{bias} \cdot R_L \tag{4.4}$$

The tail current I_{bias} is selected to ensure complete current switching between the tracking and latching pairs and also to achieve a drain current density which extracts maximum gain from the tracking pair. The output voltage swing is dictated by the successive divider circuits that the prescaler needs to drive. However, for an independent component design, a reasonable output amplitude is selected which

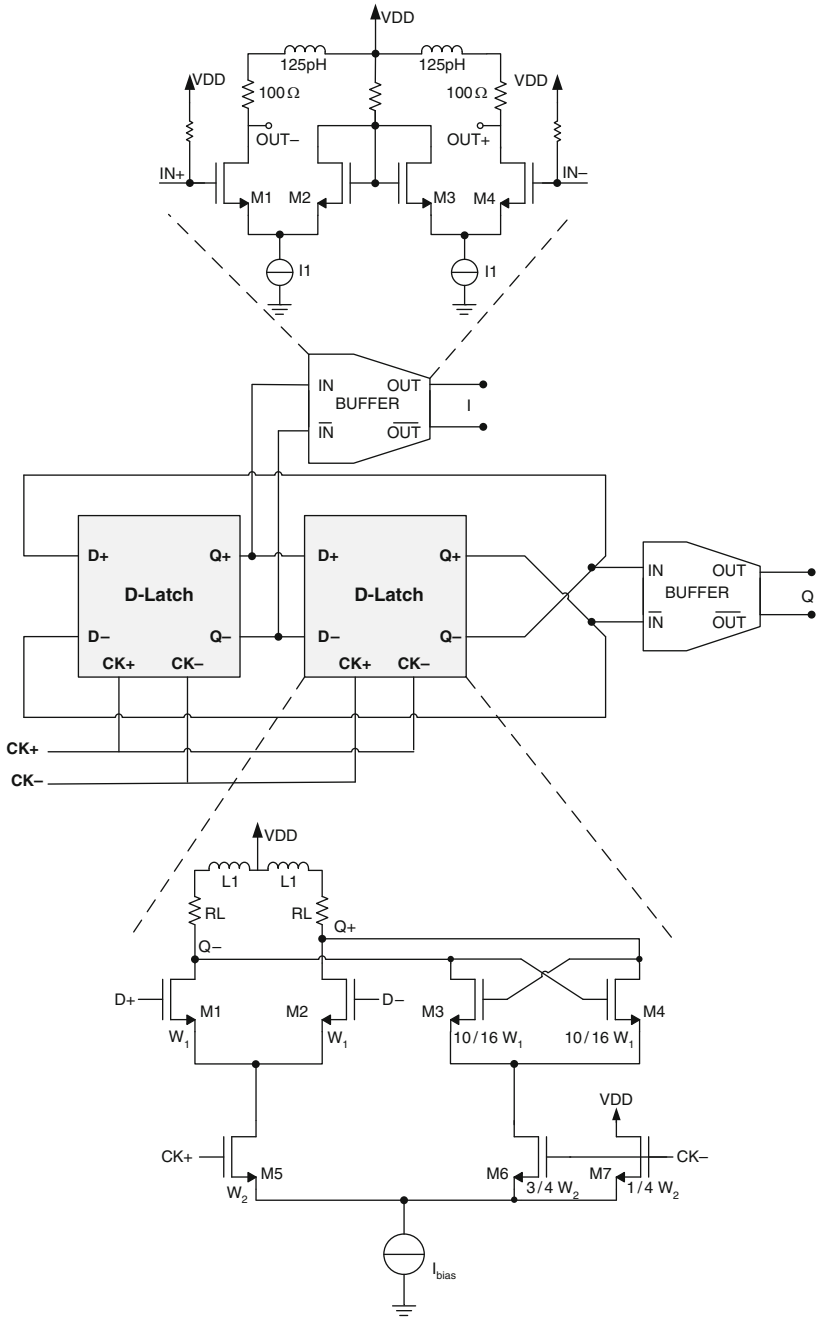

Fig. 4.11 Static frequency divider with circuit schematics of D-Latch and output buffer

could be measured reliably. The above two parameters define the tracking pair dimensions and required load resistance R_L for the D-latch and does not allow arbitrary low values to reduce the RC time constant. The total capacitance seen at the output consists of a number of contributions and can be given by

$$C_{total} \cong C_{gs,t} + C_{db,t} + 2C_{gd,t} + C_{gs,l} + C_{db,l} + 4C_{gd,l} + C_{R_L} + C_{buff} + C_{par} \quad (4.5)$$

where C_{gs}, C_{db} and C_{gd} are the gate-to-source, drain-to-bulk and gate-to-drain capacitances of the transistor and the subscript 't' and 'l' correspond to the tracking and latching pairs, respectively. C_{RL}, C_{par}, C_{buff} and are the parasitic contributions from the load resistors, layout interconnect and buffer transistors which act as external load for the divider, respectively. The factor 4 with the $C_{gd,l}$ term accounts for two differentially connected $C_{gd,l}$'s [69]. Equation (4.5) provides a number of insights to reduce the total capacitance which is exploited to achieve high frequency operation.

When the clock inputs (CK+ and CK−) are equal to a common-mode value, both the master and slave latches are semi-transparent, allowing signals to propagate through both latches. This makes the circuit work as a two stage ring oscillator with a self-oscillation frequency of $1/4\tau_{pd}$ (where τ_{pd} is given by (4.2)). Increasing the self-oscillation frequency leads to higher operation frequency of the divider. Therefore, the capacitance contributions from different sources are decreased to achieve a high self-oscillation frequency. The significant contribution from the latch transistors ($4C_{gd,l}$) motivates the investigation for its reduction. To this end, simulations are carried to determine the optimum ratio between tracking pair (M1, M2) and latching pair (M3, M4). The approach of finding the best ratio instead of absolute transistor dimensions assists in generalizing the result. The tracking pair dimensions are first selected based on the required output amplitude and tail current. The width of the latch transistors is then varied between two values, lowest being 1/16th of the tracking pair and highest being equal to it. The resulting self-oscillation frequency and output amplitude of the divider is plotted in Fig. 4.12. As the latching pair dimensions are increased the self-oscillation frequency decreases owing to increased capacitance at the output nodes. The output amplitude, although mainly defined by the tracking pair, is marginally affected by the latch pair. Initially it increases as the latch pair width is increased and after reaching a maximum it rolls-off due to excessive loading of the tracking pair. The region between 8/16 and 11/16 offers the best compromise between the two parameters and is highlighted by the dashed circle. Similar simulations done for different widths of tracking transistors yield an almost identical optimum region. It is to be noted that the SFD does not self-oscillate if the latch transistors are smaller than 1/4th of the tracking transistors as the negative resistance is too small to initiate oscillation. The positive feedback and the reduction of width of the latch pair imply that a fraction of the tail current can be sufficient for it, to take hard decision between high and low level of the output. Thus, the current for the latch pair is reduced by splitting the corresponding clock transistor into two parallel transistors M6 and M7. Parametric simulations show that using 3/4th of the tracking pair current for the latch pair provides an 8%

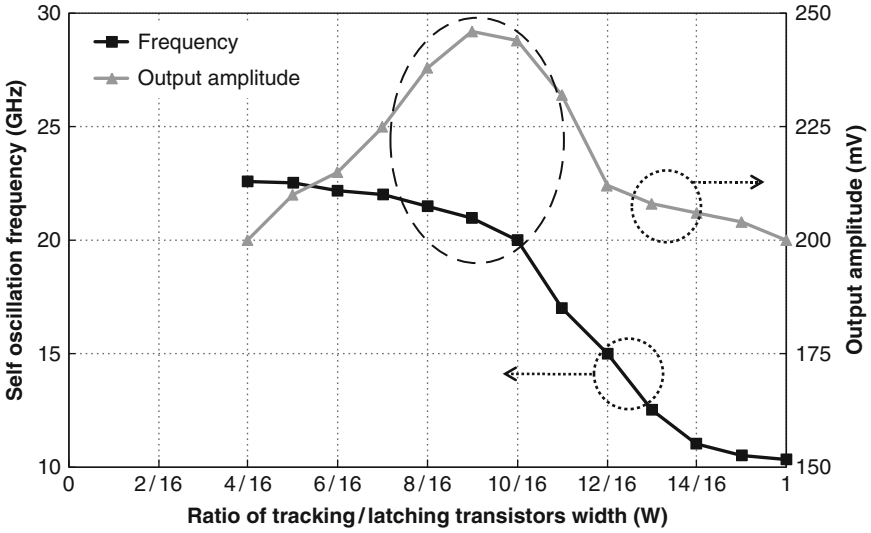

Fig. 4.12 Self-oscillation frequency and output amplitude of SFD as a function of ratio of tracking and latching transistors width (optimum area is *encircled*)

improvement in the output amplitude and does not degrade other performance parameters. Therefore, M6 and M7 distribute the current by having width of 3/4 W_2 and 1/4 W_2, where W_2 is the width of M5 providing the current to the tracking pair. The transistor M7, though wastes 1/4th of the tail current, is added to preserve the differential structure for the clock inputs and avoid any imbalance.

The second technique adopted to enhance the operation frequency of the SFD is termed as shunt peaking. This technique can be understood conceptually in time as well as frequency domain. It is known that the gain of a capacitively loaded amplifier (tracking pair in SFD case) rolls off as frequency increases because the capacitor's impedance diminishes. The introduction of an inductor in the load, generates an impedance which increases with frequency (i.e. it introduces a zero). This nullifies the decrease in impedance of the capacitor and results in a constant impedance level over a broader frequency range as compared to the original RC network. Observing the time domain impact, it can be seen that, as current cannot change instantaneously through the load resistor R_L due to the shunt peaking inductor, more current is utilized to charge the load capacitance. This decreases the rise and fall times of the SFD and thus enhances the maximum operation frequency [70].

There are several considerations for the shunt peaking inductor used in this design. As the load resistor is connected in series with the inductor, their combination determines the effective quality factor. Therefore, a high quality factor inductor is not required. This flexibility enables the use of a stacked inductor which offers the valuable advantage of smaller silicon foot-print. A high self-resonance frequency (f_{SR}) has to be maintained to ensure inductive behavior uptil the highest operation

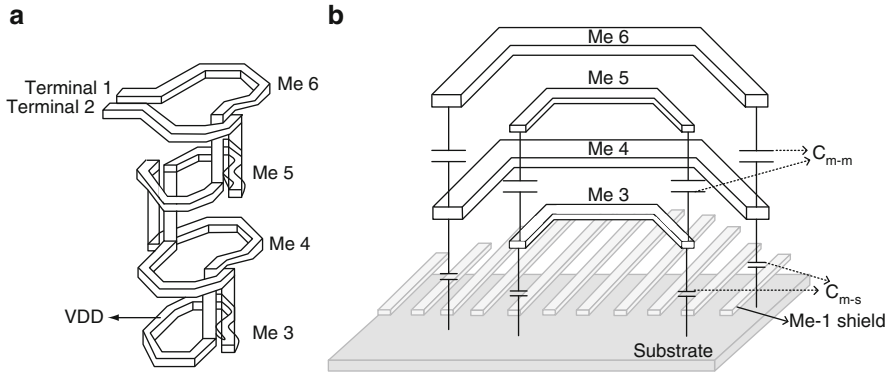

Fig. 4.13 Complete shunt peaking stacked inductor (**a**), and its cross-section showing parasitic capacitances, metal shield and substrate (**b**) [32]

frequency of the SFD. The peaking inductor L1 in Fig. 4.11 is implemented in a differential structure with the center tap connected to VDD. The available six layer metal stack is used to construct the stacked structure as shown in Fig. 4.13. Top four metals from Me6–Me3 form the inductors whereas Me1 is used below the inductors as patterned ground shielding to provide isolation from substrate.

Metal 6 winds downward with a right-half turn and is interleaved with a left-half turn on the adjacent lower metal layer. When the winding reaches Me3 it winds upward along the counter path. The consecutive layers, for instance Me6 and Me5 are offset by a metal width, so that the loops on Me6, Me4 and Me5, Me3 are identical. This approach eliminates the parasitic capacitance between adjacent metal layers. The metal to substrate capacitance is also limited to Me3 and further reduced by using Me1 as a shielding layer. An optimum value of 125 pH for the shunt peaking inductor is required based on a series of AC and transient simulations. In order to estimate the self resonance frequency of the inductor, the total parasitic capacitance of the structure is calculated based on the distributed capacitance model (DCM) [71, 72].

The DCM model analytically calculates the different parasitic capacitances of the inductor by using the voltage distribution (also called voltage profile) over the inductor. It assumes that firstly, voltage distribution is proportional to the length of the metal track and secondly, the voltage potential is equal in each half turn of the inductor and is determined by averaging the voltages of the previous half turn and the next one. For an n turn inductor, each half turn be denoted as $l_1, l_2, \ldots, l_{2n}$, the metal width as W, metal-to-metal overlap capacitance as $C_{m\text{-}m}(k)$ and metal-to-substrate capacitance as $C_{m-s}(k)$, we can define

$$d_k = \frac{\sum_{i=1}^{k} l_i}{\sum_{i=1}^{2n} l_i} \tag{4.6}$$

and the voltage of the kth half turn is given by

$$V(k) = \frac{1}{2} V_0 [1 - d(k-1) - d(k)] \tag{4.7}$$

where V_0 is the peak voltage across the inductor. The total electrical energy stored in the inductor is divided into two parts: one is in the energy stored in metal-to-substrate parasitic capacitor E_{m-s} and the second in the metal-to-metal capacitor E_{m-m} and can be expressed as

$$E_{total} = \frac{1}{2} C_{total}\, V_0^2 = E_{m-s} + E_{m-m} = \frac{1}{2} C_{m-s}\, V_0^2 + \frac{1}{2} C_{m-m}\, V_0^2 \tag{4.8}$$

To determine E_{total}, the two parasitic capacitance C_{m-s} and C_{m-m} have to be calculated. To this end, it can be observed that metal to substrate capacitance is limited to the lower two metals only and the energy stored can be given as

$$\begin{aligned} E_{m-s} &= \frac{1}{2} \sum_{k=n}^{n+1} C_{m-s}(k)\ \cdot l_k \cdot W \cdot V^2(k) \\ &= \frac{V_0^2}{8} \sum_{k=n}^{n+1} C_{m-s}(k)\ \cdot l_k \cdot W \cdot [1 - d(k-1) - d(k)]^2 \end{aligned} \tag{4.9}$$

and comparing it to (4.8) gives

$$C_{m-s} = \frac{1}{4} \sum_{k=n}^{n+1} C_{m-s}(k)\ \cdot l_k \cdot W \cdot [1 - d(k-1) - d(k)]^2 \tag{4.10}$$

On the other hand, the energy stored in metal-to-metal capacitors is given by

$$\begin{aligned} E_{m-m} = &\frac{1}{2} \sum_{k=1}^{n-2} C_{m-m}(k)\ \cdot l_k \cdot W \cdot [V(k) - V(k+2)]^2 \\ &+ \frac{1}{2} \sum_{k=n+1}^{2n-2} C_{m-m}(k)\ \cdot l_k \cdot W \cdot [V(k) - V(k+2)]^2 \end{aligned} \tag{4.11}$$

The two summations correspond to the capacitance during winding-down and winding-up of the inductor. Using (4.7), the above equation can be re-written as

$$\begin{aligned} E_{m-m} = &\frac{V_0^2}{8} \sum_{k=1}^{n-2} C_{m-m}(k)\ \cdot l_k \cdot W \cdot [d(k+2) - d(k) + d(k+1) - d(k-1)]^2 \\ &+ \frac{V_0^2}{8} \sum_{k=n+1}^{2n-2} C_{m-m}(k)\ \cdot l_k \cdot W \cdot [d(k+2) - d(k) + d(k+1) - d(k-1)]^2 \end{aligned} \tag{4.12}$$

and the corresponding C_{m-m} can be extracted as

$$C_{m-m} = \frac{1}{4}\sum_{k=1}^{n-2} C_{m-m}(k)\ \cdot l_k \cdot W \cdot [d(k+2) - d(k) + d(k+1) - d(k-1)]^2 + \frac{1}{4}\sum_{k=n+1}^{2n-2} C_{m-m}(k)\ \cdot l_k \cdot W \cdot [d(k+2) - d(k) + d(k+1) - d(k-1)]^2 \tag{4.13}$$

Combining (4.10) and (4.13) yields the total capacitance of the structure

$$C_{total} = \frac{1}{4}\sum_{k=n}^{n+1} C_{m-s}(k)\ \cdot l_k \cdot W \cdot [1 - d(k-1) - d(k)]^2 + \frac{1}{4}\sum_{k=1}^{n-2} C_{m-m}(k)\ \cdot l_k \cdot W \cdot [d(k+2) - d(k) + d(k+1) - d(k-1)]^2 + \frac{1}{4}\sum_{k=n+1}^{2n-2} C_{m-m}(k)\ \cdot l_k \cdot W \cdot [d(k+2) - d(k) + d(k+1) - d(k-1)]^2 \tag{4.14}$$

$C_{m-s}(k)$ and $C_{m-m}(k)$ in the above equation is found using relative dielectric constant of the respective metal layer whereas other parameters depend on the length and width of metal traces of the inductor. The total capacitance of the stacked inductor is calculated to be 37.5 fF. This yields a self resonance frequency of 73.5 GHz which is high enough for its usage as a shunt-peaking inductor:

$$f_{SR} = \frac{1}{2\pi\sqrt{LC_{total}}} = 73.5\ \text{GHz} \tag{4.15}$$

The output buffer which is needed for measurement purposes generates another parasitic capacitance contribution in (4.5) represented by C_{buff}. In order to reduce the input capacitance of the buffer and decrease the loading at the output nodes of the divider, an f_T doubler stage (transistor M2 and M3) is added to a standard differential amplifier as shown in Fig. 4.14. For a differential input, the device capacitances appear in series with each other, which halves the effective C_{gs} capacitance as compared to a differential stage. The f_T doubler approach increases the unity-gain frequency $f_T = g_m/2\pi\ (C_{gs} + C_{gd})$ of the devices and the bandwidth of the buffer as well [73]. The drawback of this approach is the extra current required for the two differential amplifiers. The compact shunt-peaking inductor designed in the divider is also re-used in the buffer without significant area penalty. The simulated −3dB bandwidth of the buffer is increased from 22.6 to 57.8 GHz due to the f_T doubler stage and shunt peaking.

Owing to the differential design in both the divider and buffer, the layout is kept as symmetric as possible. The quadrature outputs from the buffer are matched to the

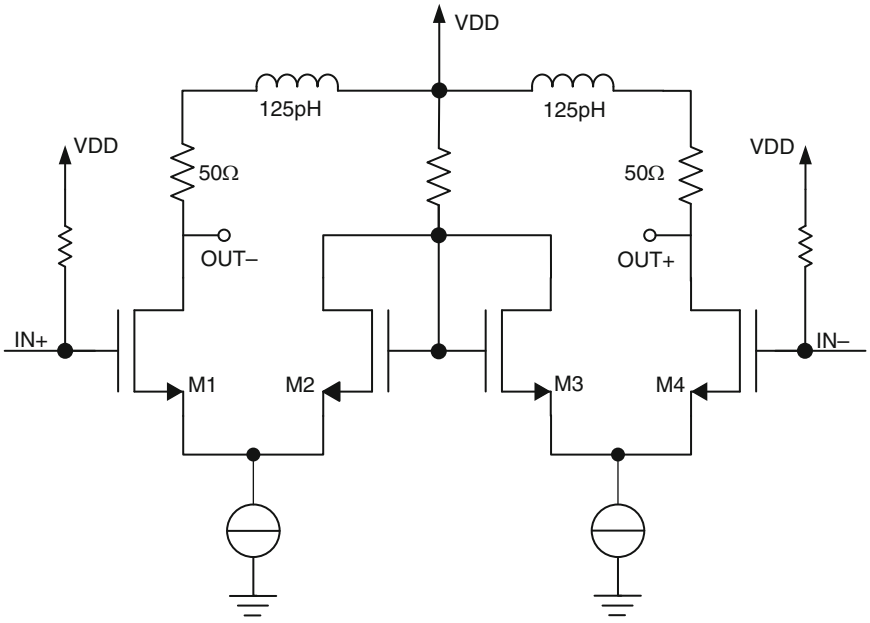

Fig. 4.14 Output buffer for static frequency divider

measurement equipment by using 50 Ω transmission lines to the bond pads. The circuit is fabricated in a 90 nm, bulk CMOS, LP technology, with six metallization layers. Due to bond pad limitations the chip area is 900 × 700 μm^2. However, the active area is less than half of the above value. The chip micrograph is shown in Fig. 4.15.

The SFD was measured on wafer with high frequency differential probes (GSGSG). A 180° hybrid provides the required anti-phase clock inputs. The measured input sensitivity of the SFD which plots the minimum input power required, as a function of input frequency is plotted in Fig. 4.16. The losses from the measurement setup have been de-embedded. The simulated sensitivity curves for the divider with and without shunt-peaking are also presented. It can be seen that shunt-peaking improves the maximum operation frequency from 29 to 43 GHz which is a 1.48 times improvement. This is close to the theoretical maximum enhancement (1.7 times) using shunt-peaking [70]. The measured maximum frequency of 35.5 GHz lies between the two simulated curves. The divider can operate from 2 to 35.5 GHz with an input power below +1dBm. The maximum frequency division is achieved at a power consumption of 14.4 mW per D-latch from a 1.2 V power supply. Each output buffer consumes 9.6 mW and the total power consumption is 48 mW. The circuit was unable to hit the target frequency of 40 GHz and the considerable shift in frequency, after investigation, is attributed to inaccurate device models which were only characterized uptil 20 GHz.

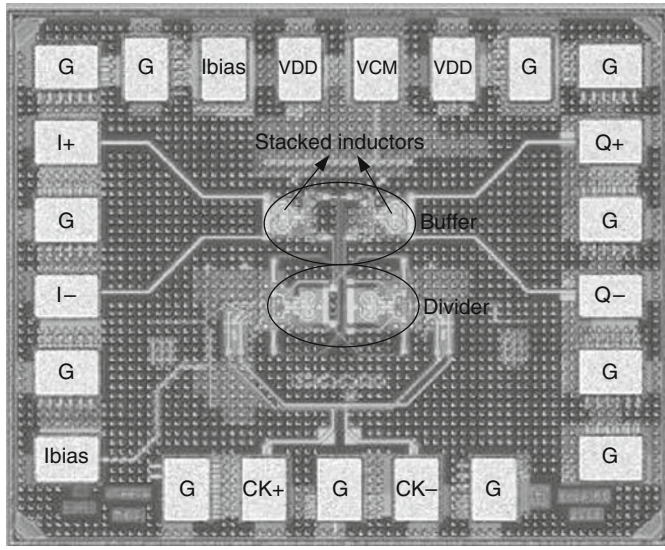

Fig. 4.15 Chip micrograph of the SFD

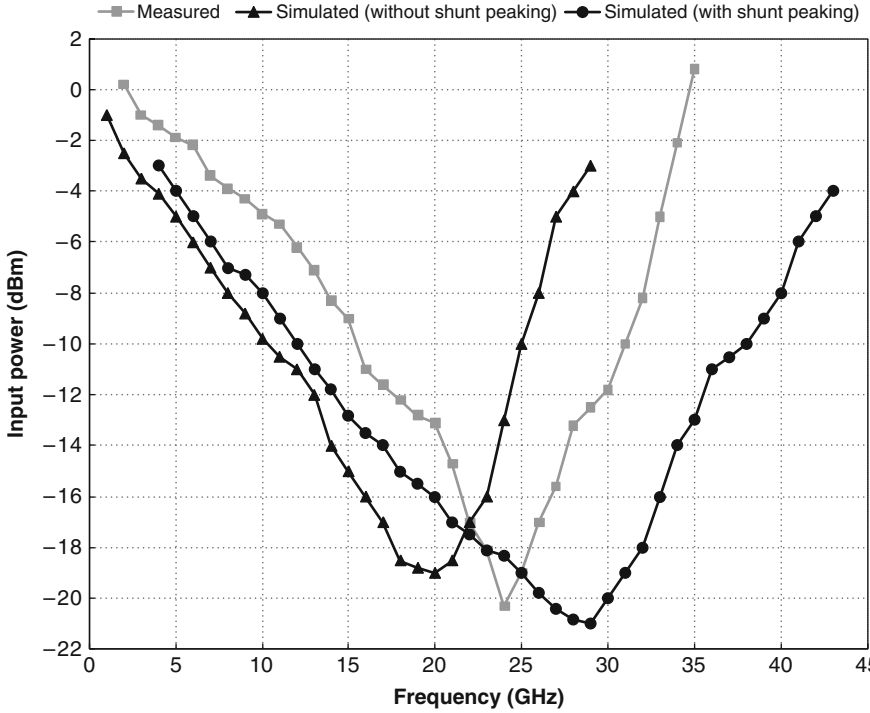

Fig. 4.16 Simulated and measured input sensitivity curves

The measured output spectrum at maximum frequency of operation is shown in Fig. 4.17. The measured phase noise of the divider output is −124.6 dBc/Hz at 1 MHz offset from the carrier (for an input CLK of 30 GHz). The input phase noise of the generator is −119.4 dBc/Hz which is close to the 6 dB theoretical difference due to frequency division.

4.1.3 40 GHz Divide-by-2 ILFD

The inability of the static frequency divider presented in the preceding section to reach the target frequency of 40 GHz, points to investigation of an alternative prescaler architecture for the same purpose. The natural choice is an injection locked frequency divider which has been demonstrated at mm-wave frequencies, albeit with narrow locking range. Circuit techniques are employed in this work to address the latter characteristic and satisfy locking range requirements for the proposed synthesizer.

As mentioned in Section 4.1.1, injection locking or pulling is a special type of oscillation where a free running oscillator is forced to oscillate at an injection frequency (f_{inj}) which different than its self-oscillation frequency (f_0). When f_{inj} is quite different from from f_0, "beats" of the two frequencies are observed. As it approaches f_0, the beats start to decrease and when f_{inj} enters a certain range close to f_0, the beats disappear and the oscillator starts to oscillate at f_{inj} instead of f_0. The frequency range in which injection locking occurs is called locking range (LR). Injection locking also occurs if f_{inj} is close to a harmonic or sub-harmonic of f_0, i.e. nf_0 or f_0/n. This characteristic is utilized to design injection locked frequency dividers or multipliers, respectively, as shown in Fig. 4.18. As an example, in case of a divide-by-2 frequency divider, frequencies close to the second harmonic of f_0 are injected to achieve a locked output at the oscillation nodes which is exactly

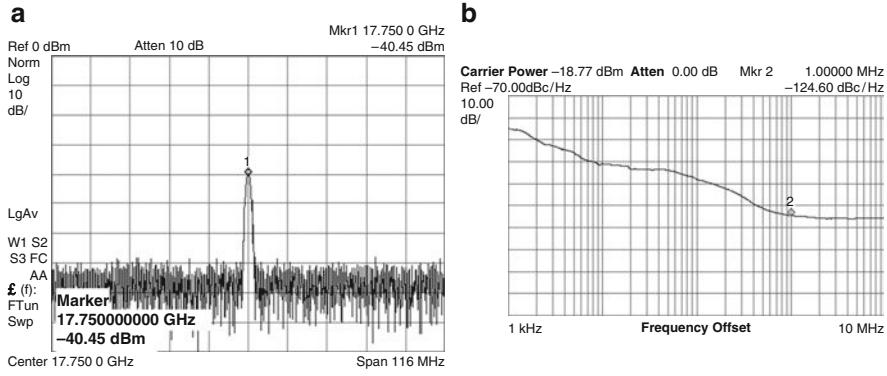

Fig. 4.17 SFD measured results: spectrum at maximum frequency (**a**), and phase noise (**b**)

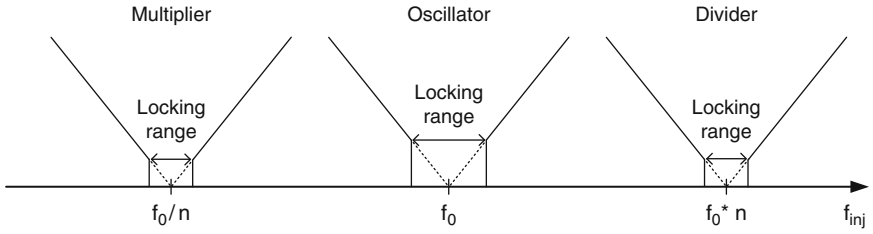

Fig. 4.18 Injection locking to achieve oscillator (*center*), divider (*right*) and multiplier (*left*)

half the injected frequency. The strength of harmonics in a non-linear oscillator is always lower than the fundamental, which manifests itself in reduced locking range when it is used as a divider or multiplier as compared to an injection locked oscillator only (for identical injection power). This is graphically shown in Fig. 4.18.

The limited locking range in ILFDs is of main concern and in order to address this issue, its dependencies on circuit parameters have to be investigated and will be considered next. The locking range of ILFDs has been treated extensively during many studies of injection locking of oscillators over the last 60 years. Adler [74] introduced the first expression for locking range in 1946 as

$$\left|\frac{\Delta f}{f_0}\right| \leqslant \frac{1}{2Q}\,\frac{V_{inj}}{V_0} \tag{4.16}$$

where Δf is the range of frequencies around the free-running oscillation frequency f_0, Q is the quality factor of the tank and V_{inj} and V_0 are voltages of the external injected signal and the oscillator, respectively. In [75, 76], the injection locking oscillator is treated as a non-linear function to derive the following locking range expression

$$\left|\frac{\Delta f}{f_0}\right| \leqslant \frac{H_0\, a_2\, V_{inj}}{2Q} \tag{4.17}$$

where Δf, f_0, Q and V_{inj} are the same as before, H_0 is the impedance of the RLC tank at resonance and a_2 is the second-order coefficient of the nonlinear function.

In order to simplify the analysis, [59] adopts a time-variant view as opposed to a non-linear approach to derive a locking range expression for an injection locked oscillator given by

$$\frac{\Delta f}{f_0} = \frac{1}{2Q}\cdot\frac{I_{inj}}{I_{osc}}\cdot\frac{1}{\sqrt{1-\frac{I_{inj}^2}{I_{osc}^2}}} \tag{4.18}$$

which in case $I_{inj} << I_o$ can be simplified to

$$\frac{\Delta f}{f_0} \approx \frac{1}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \tag{4.19}$$

where I_{osc} and I_{inj} are the oscillator and injection current, respectively. The application of the above equation to an ILFD can be understood by considering a conventional divide-by-2 ILFD shown in Fig. 4.19a in which the injection signal is at approximately twice the self-oscillation frequency f_0. After voltage to current conversion I_{inj} reaches the common-source node P of the cross-coupled pair (M1–M2). This pair can also be considered as a mixer where the two currents (I_{inj} and I_{osc}) are mixed, down-converting f_{inj} to $f_o \pm f_{inj}$, and the sum component is suppressed due to tank selectivity. Assuming abrupt switching of M1 and M2, the injection of I_{inj} at f_{inj} into node P can be considered equivalent to injection of I_{inj} $2/\pi$ at $f_{inj} - f_0$ into the LC tank, where $2/\pi$ is the mixer conversion gain. As $f_{inj} - f_0 \approx f_0$, the divide-by-2 operation is achieved and the locking range of (4.19) can be re-written as

$$\frac{\Delta f}{f_0} \approx \frac{1}{2Q} \cdot \frac{2}{\pi} \cdot \frac{I_{inj}}{I_{osc}} \tag{4.20}$$

It is also to be noted that due to the differential topology, the non-linearity of M1 and M2 (switching pair) has odd-symmetry. Therefore, only mixing products of odd numbers are generated which correspond to even division ratios, i.e.

$$f_{inj} - (2n-1)f_o = f_o \tag{4.21}$$

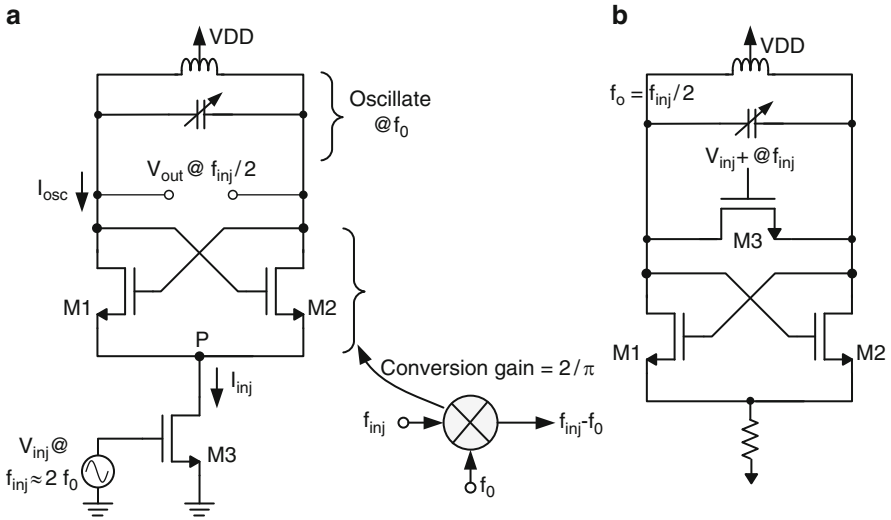

Fig. 4.19 Conventional ILFD with injection at tail-node and comparison with a mixer (**a**), and direct injection-locked frequency divider (**b**)

where n = 1, 2, 3,. . . and n = 1 corresponds to divide-by-2 ILFD. Higher division ratio (4, 6, . . .) ILFDs can also be designed using the same topology.

Revisiting the locking range expressions in (4.16), (4.17) and (4.20), it is clear that for larger LR, the quality factor (Q) of the LC tank should be minimized. This is because smaller Q values correspond to wider band-pass bandwidths for the LC tank and decrease the tank selectivity. The second important dependency of LR is on the injection voltage (V_{inj}) or injection current (I_{inj}), the improvement of which increases the locking range. At this point, it is useful to distinguish between the internal and external injection signals. In the implementation of Fig. 4.19a, the input signal is injected to the gate of M3 whereas the internal injection point is the common-source node P. Although increasing one increments the other as well, the locking range is predominantly defined by the effective injection power reaching the oscillator core. Therefore, the LR can be enhanced by maximizing the internal injection power while using the same external injection, i.e. by alleviating the loss mechanisms which reduce the power from the external to internal injection points. As an example, we can see that the circuit in Fig. 4.19a has considerable parasitic capacitance at node P constituted by C_{gd} and C_{db} of M3 and C_{sb} of both M1 and M2. In addition, as the injection transistor M3 has a biasing function in the circuit, the required width of the transistor is usually large, thus increasing the parasitic capacitances. To remedy the loss of injection power in the parasitic capacitance, a shunt peaking inductor can be used to resonate out this capacitance at the injection frequency f_{inj} [66]. However, this solution has the disadvantage of extra silicon area required for the shunt peaking inductor.

Therefore, in order to improve the internal injection power, a different injection point is selected in this work. Termed as “direct” or “tank” injection, the input injection transistor is placed across the LC-tank as shown in Fig. 4.19b. There are a number of evident advantages of this scheme. Firstly, the parasitic capacitance is only limited to the injection transistor M3 which can be designed much smaller than the injection transistor in the conventional topology, as it does not have any biasing function. Thus, the injection efficiency is improved resulting in larger locking range. Secondly, due to the differential output of VCOs, differential injection is required in the prescaler to equally load the VCO outputs. In comparison to the conventional design, where a dummy injection transistor would be required to achieve this, the direct injection offers a much simpler solution by adding a PMOS injection transistor across the tank with its gate connected to the second VCO output [67].

The proposed synthesizer requires quadrature outputs from the prescaler which are spaced 90° apart. The conventional and the direct-injection ILFD both provide differential outputs only, so a change in circuit implementation is necessary. One option is to employ a passive poly-phase filter after the ILFD to generate the quadrature outputs. This approach has two main drawbacks. Firstly, a power hungry buffer would be needed between the ILFD and filter to avoid loading affects and this would result in phase noise degradation. Secondly, variations in the RC values (in the order of 15–25%) of the filter would require many tuning stages to achieve acceptable quadrature accuracy. An alternative to the poly-phase filter

approach, used in this work, can be understood by Fig. 4.20 (square pulses are used for simplicity). It can be noted that a phase change of 180° at f_{inj} corresponds to a phase change of 90° at $f_{inj}/2$, as the signal width is double at the latter frequency. Therefore, using this concept at circuit level, the quadrature outputs can be obtained by injecting the differential (180° spaced) VCO outputs to two identical direct-injection ILFD stages as shown in Fig. 4.21. The 20 GHz differential I-Q outputs from the prescaler are used for the second down-conversion in the sliding-IF architecture as well as for the direct-conversion architecture using a tripler (which requires differential I-Q as input).

The main concern of the ILFD of Fig. 4.21 is the accuracy of the I-Q outputs. Although both ILFD stages can be designed and laid-out identically, still the relative PVT variations for one stage (or active/passive components) could be

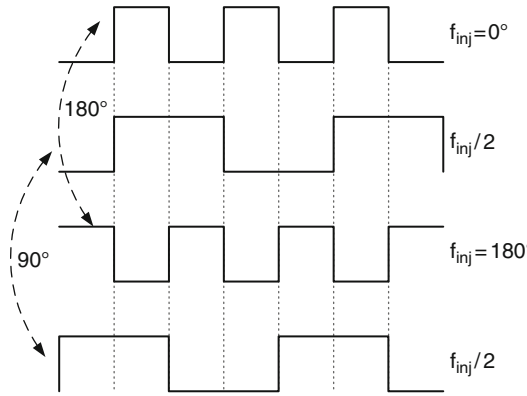

Fig. 4.20 Generation of 90° spaced ILFD outputs by changing the input injection phase by 180°

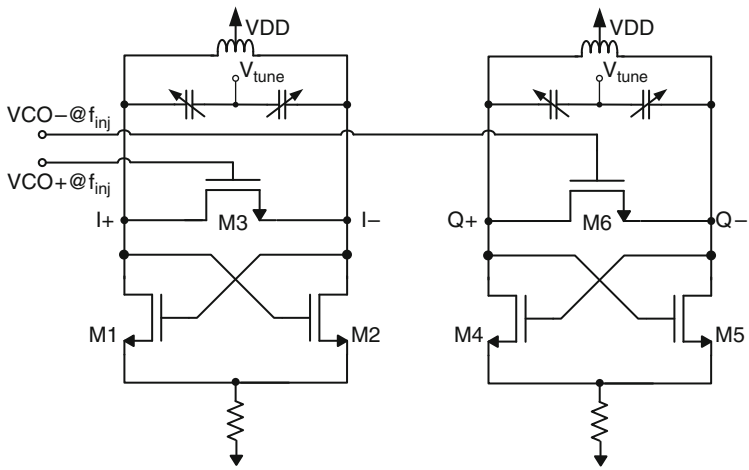

Fig. 4.21 Quadrature ILFD using differential VCO output

different from the other, resulting in I-Q mismatch. To address this issue, the two ILFD stages are coupled to each other to force them to run in quadrature as shown in Fig. 4.22. The coupling, called parallel or anti-phase coupling [77], is achieved by connecting each oscillator output to the other oscillator with transistors M7–M10 in parallel to the cross coupled transistors M1, M2 and M4, M5. To understand the forced quadrature operation of this setup, it can be noted that each ILFD stage can be modeled as a gain stage. Also, for any oscillator structure with feedback, the loop phase must be 0° or 360°. Thus, since the crossed connection (due to anti-phase coupling) between the two ILFDs represent a phase shift of 180°, the two stages must have an additional phase shift of 180°. Hence, the phase shift across one stage is 90° ensuring quadrature operation.

The source terminals of the coupling transistors are connected to the common-source nodes of the cross-coupled pairs to alleviate the need of a separate current source, in other words the current is shared between both coupling and cross-coupled pairs. In comparison, to the series (or cascade) coupling presented in [78], which requires large coupling transistors and voltage head-room due to stacked structure, this architecture employs smaller coupling transistors reducing the additional parasitic capacitance. Thus, the LC-tank is minimally affected. The optimized dimensions of the coupling transistors are determined by running transient and noise simulations to extract the best performance in terms of output power, locking range and phase noise.

The injection signal is AC-coupled to the gates of M3 and M6 using on-chip MIM capacitors whereas the DC-bias is obtained by using a resistive divider. The use of inductors makes it unavoidable to use long interconnects from the bondpads to the injection transistors. As shown in Fig. 4.24a, coplanar transmission lines are used where space is available. However, close to the core, the interconnect has to traverse a length of ∼78 μm and space limitation does not allow the use of coplanar TLs. Due to the capacitive input of the injection transistors, there is an inherent

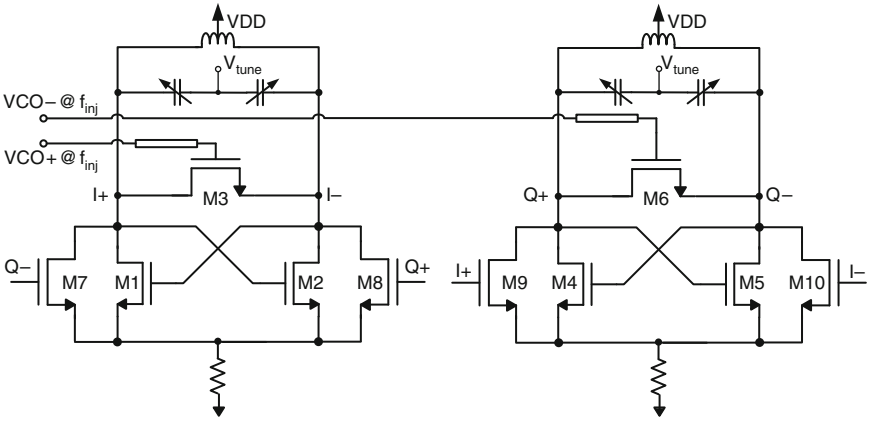

Fig. 4.22 Forty gigahertz direct injection I-Q ILFD using anti-phase coupling

power mismatch between the gate input and the signal generator equipment. Consequently, at high frequencies, part of the injection signal is "eaten-up" by the parasitic input capacitance. A useful solution adopted in this work, is to utilize the required interconnect for power matching at the input of the injection transistor. The interconnect is implemented as a micro-strip transmission line and shielded in a cavity-like structure similar to Fig. 3.7. Cadence^{TM} parametric simulations are used to determine the required inductance for maximum power matching. After optimization, EM simulations are done in ADS Momentum to determine the inductance per unit length for different metals in the technology stack as shown in Fig. 4.23. The metal layer Me3, which is closest to the required value is used in the interconnect layout for input injection. Due to this injection enhancement technique, input sensitivity is improved and for the same output power, the required input signal power is almost halved.

The ILFD is designed in a 65 nm Taiwan Semiconductor Manufacturing Company (TSMC) bulk CMOS technology having six metallization layers. The top layer (Me6) is ultra-thick and specifically suited for inductor design. The inductors of the two ILFD stages are a single turn, top-metal symmetric octagonal structure. The center-tap is connected to the voltage supply. The width of the metal trace is 9 μm with an inner radius of 63 μm. The guard-ring around the inductor is placed 10 μm away from the signal trace and area of the inductor is 209 × 188 μm^2. The resulting inductance at 20 GHz is 310 pH with a Q-factor of ∼25.

Although the simulated locking range covers the required frequency range of 38–42 GHz, still keeping in mind the expected shift due to layout parasitics and

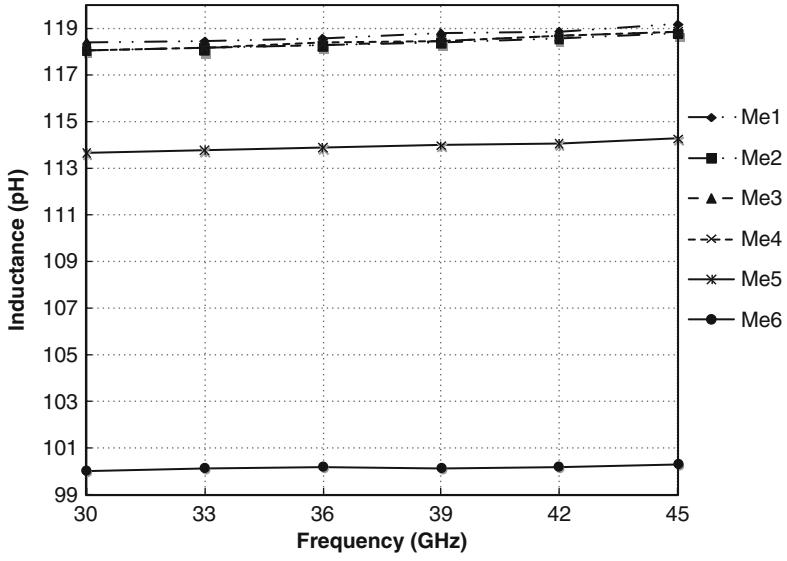

Fig. 4.23 Inductance of a 2.5 μm wide, 78 μm long interconnect in different metal layers

PVT variations, varactors are employed in order to compensate this shift. Using varactor tuning increases the locking range indirectly and can provide extra flexibility in the synthesizer. The varactors are accumulation MOS (A-MOS, discussed in Section 4.2.3 in more detail) type and two of them are connected back-to-back to provide a common-mode node for tuning. To decrease the series resistance, the varactors are chosen to have multiple fingers. The width and length per finger is 2.1 μm and 300 nm respectively with 28 fingers in total. The resulting capacitance and Q-factor for a tuning voltage of 0–1.2 V is 128–34 fF and 5–18, respectively. The optimized width of coupling transistors M7–M10 is 7.5 μm and is one-fourth of the cross-coupled transistors M1–M4 (30 μm). The injection transistors M3 and M6 are 9 μm wide with minimum channel length. The 150 Ω polysilicon based resistors in the tail node provide common-mode rejection and define the DC through the ILFD. Differential common-source output buffers are employed for measurement purposes and matched to a 50 Ω environment.

The chip micrograph is shown in Fig. 4.24a. Due to differential I-Q outputs, two output pads as well as a differential input pad (GSGSG) are required, whereas the fourth side is dedicated for DC inputs. The core circuit consisting of transistors, varactors and output buffers is placed in close proximity between the two inductors. The bond-pad limitation necessitates the need for long interconnects from the bond-pads to the active circuit and vice versa. To reliably transfer the high frequency signals, 50 Ω transmission lines are utilized at both the input and output terminals. The transmission line structure is similar to the one explained in Section 3.1.3. The signal trace and ground plane are 5 and 10 μm wide respectively, whereas the spacing between them is 4.22 μm. The ground plane consists of all metal layers connected through large number of vias as well as substrate contacts to ground. All the vacant chip area is covered with ground meshing similar to the one in Section 3.1.4. The total chip area is 900 × 750 μm^2. The divider is measured by on-wafer probing using the setup shown in Fig. 4.24b. The input 40 GHz signal from an

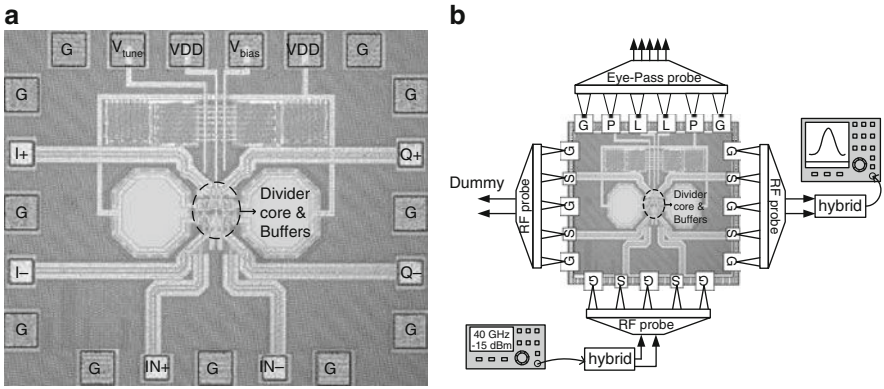

Fig. 4.24 Forty gigahertz ILFD chip micrograph (**a**), and measurement setup (**b**)

Agilent signal generator is applied to a single-to-differential converter (180° hybrid) and then passed on the RF probe. The output differential signal is converted to single-ended using a similar hybrid and observed by an Agilent spectrum analyzer (E4446A). The phase noise is also measured by the spectrum analyzer (SA).

The free-running frequency of the inherent oscillator is first measured by switching "off" the injection signal. It starts oscillating at 1V supply and the maximum tuning range from 17.5 to 20.8 GHz is obtained with a 1.2 V supply. After fixing the tuning voltage of the varactor to a certain value, the injection signal is switched "on" close to double the self-oscillating frequency for that particular V_{tune}. The input power is reduced to determine the minimum value for which the ILFD still locks to the input signal. This step is repeated for different input frequencies and the maximum and minimum are determined for this V_{tune}. Similarly, input sensitivity for different varactor tuning voltage are measured, three of which are plotted in Fig. 4.25. The losses of the input and output cables, connectors and hybrids are de-embedded using a "through" structure from an impedance standard substrate (ISS). The simulated sensitivity curves are also plotted for reference and match closely to the measured curves. The ILFD can operate from 30.3 to 44 GHz (14 GHz or 37% locking range). The locking range for one tuning voltage is about 6 GHz which easily satisfies the specifications. The improved injection efficiency due to direct injection topology and optimized design, results in the required input power close to free-running frequency of the ILFD to be as low as −38 dBm. The low voltage operation of the ILFD is also verified by reducing the supply voltage. The measured locking ranges for 1.1 and 1 V are 11.5 and 8 GHz, respectively. The combined power consumption of the I-Q dividers is 9 mW from a 1.2 V supply, whereas the two output buffers consume 12 mW in total. The screen-shots of maximum and

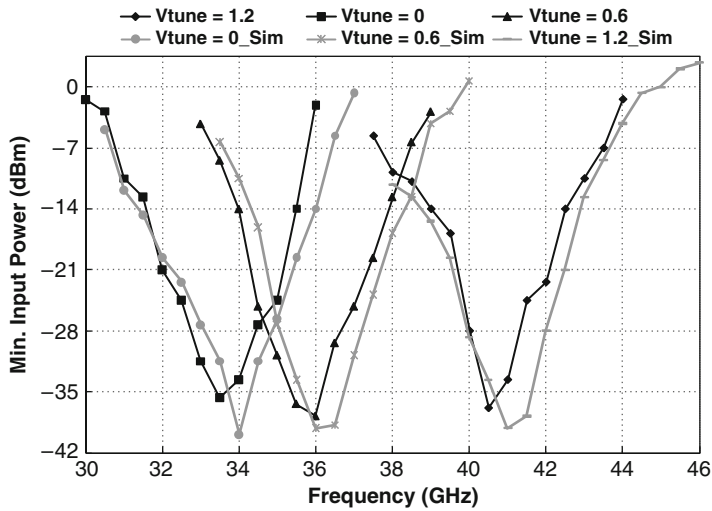

Fig. 4.25 Input sensitivity of 40 GHz divide-by-2 I-Q ILFD. Simulated (*grey*), measured (*black*)

minimum operation frequency are shown in Fig. 4.26. The phase noise of the ILFD is measured for different input frequencies. At a locked output frequency of 18.95 GHz, the measured phase noise is −131.6 dBc/Hz at 1-MHz offset from the carrier as shown in Fig. 4.27. The phase noise of the signal generator at double the frequency is −125 dBc/Hz which is close to the theoretical 6 dB difference due to frequency division. The phase noise variation of the ILFD within the complete operation range is ±2.5 dB.

The 40 GHz divide-by-2 ILFD presented above satisfies the synthesizer specifications laid out in Section 2.6 along with some margin. The required locking range was 38–42.3 GHz which is covered by this design. The measured average phase noise of the ILFD is also lower than the specified −106 dBc/Hz at 1 MHz offset.

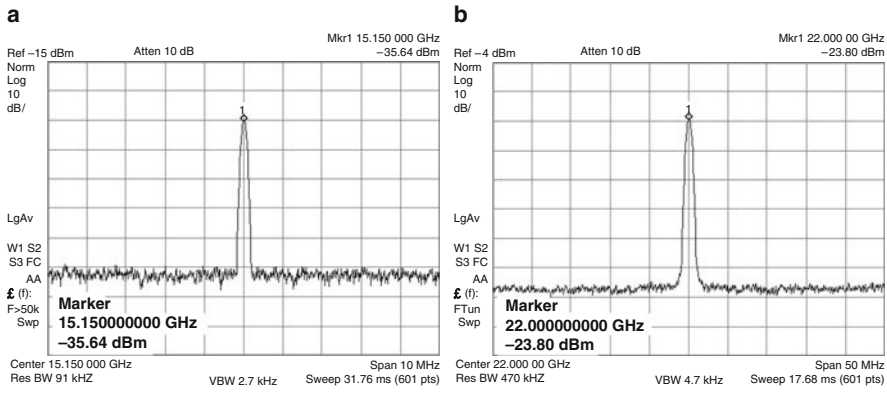

Fig. 4.26 Forty gigahertz ILFD screen-shots: minimum frequency (**a**), and maximum frequency (**b**)

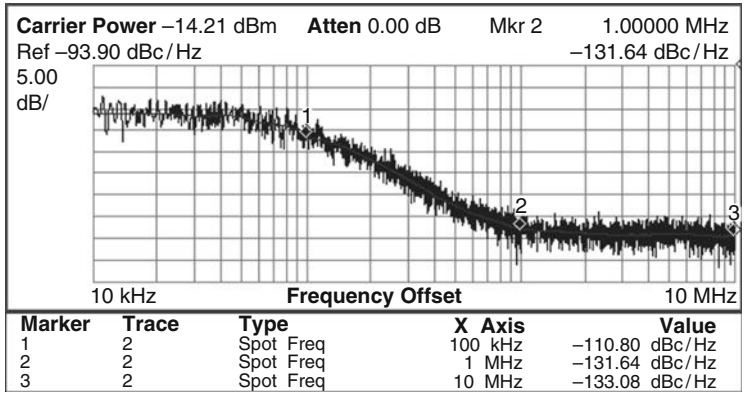

Fig. 4.27 Forty gigahertz divide-by-2 ILFD phase noise at 18.95 GHz locked output

4.1.4 60 GHz Divide-by-3 ILFD

This section discusses the next high frequency component of the proposed synthesizer (Section 2.3), which is the divide-by-3 prescaler (This work, published in [79], was carried out in cooperation with X.P. Yu, who is the first author of this publication). This prescaler is required for the direct-conversion synthesizer where the VCO is operating at 60 GHz and the divided frequency is provided to the re-usable back-end of the synthesizer. Conventionally, odd division ratios higher than 2 have been achieved by ring oscillator based frequency dividers [61]. The delay cells employed in such dividers aim to reduce the propagation delay to achieve high frequency operation. Each cell is usually composed of inverter stages which can have complementary, only-NMOS or differential structure. Such dividers, although simple to design, entail a number of concerns at mm-wave frequencies. Firstly, the operation frequency is limited to ~20GHz as the propagation delay and loop gain requirements contradict each other. Secondly, the phase noise performance of such dividers is worse as compared to LC based frequency dividers and lastly, unwanted harmonic components are more prominent in these dividers and degrade the spectrum purity of the output signal.

An alternative approach, proposed in [60], modifies the LC based injection locked frequency divider presented in the preceding section to achieve divide-by-3 frequency division. As explained by Fig. 4.19 and (4.21), only odd-order non-linearity of the cross-coupled pair (mixer stage) is present which corresponds to even numbered division ratios. In order to preserve the even-order non-linearity which would generate odd division ratios, modification in the circuit is required. To this end, it is noted that by separating the common-source node P and adding a differential amplifier as a transimpedance stage, the circuit of Fig. 4.19 can successfully preserve the even-order non-linearity. Shown in Fig. 4.28, this structure

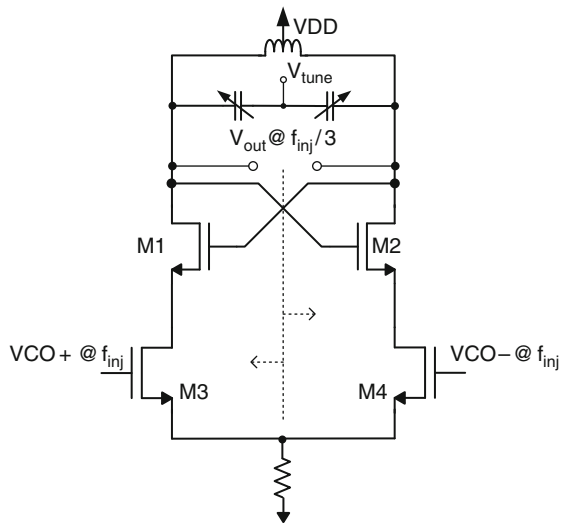

Fig. 4.28 Divide-by-3 ILFD by preserving the even-order non-linearity of M1–M2

can be viewed as two separate single-balanced mixers on either side of the dotted line. The expression relating the injection and output frequencies is be given by

$$f_{inj} - 2n \cdot f_o = f_o \tag{4.22}$$

where n = 1, 2, 3. . . and n = 1 corresponds to a divide-by-3 ILFD. As in the case of conventional divide-by-2 ILFD, the locking range of this architecture is small as the external and internal injection points are different due to which injection efficiency is degraded. As an example, the divider in [60] demonstrates a locking range of 1 GHz and an extended operation range of 3.2 GHz by employing varactors. For the synthesizer operating at 60 GHz, the required locking range of the prescaler is 6.6 GHz (Section 2.6). Therefore, injection enhancement techniques are investigated for this circuit to achieve the target locking range. This will be explained next.

The free running oscillator part of the ILFD is a complementary cross coupled architecture as shown in Fig. 4.29. As compared to an oscillator with NMOS transistors only, the complementary structure provides higher transconductance at a given current, which results in faster switching and larger output amplitude. In addition, it demonstrates superior rise- and fall-time symmetry resulting in less up-conversion of 1/f noise [80]. The active part consists of transistors M1–M4

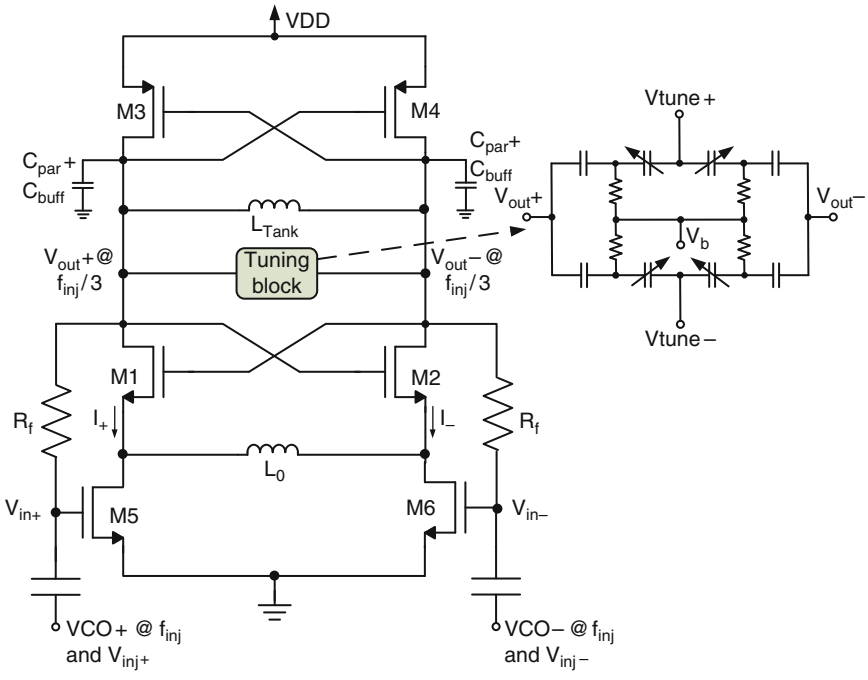

Fig. 4.29 Sixty gigahertz divide-by-3 ILFD with resistive feedback

to un-damp the load tank formed by a top-metal single turn inductor (L_{Tank}) and a capacitive part consisting of firstly, a tuning circuit composed of accumulation-MOS varactors and MIM capacitors and secondly, parasitics of the transistors (C_{par}) and output buffer (C_{buff}). The latter is added to enhance the quality factor of the varactors which is a limitation at RF frequencies and will be explained further in Section 4.2.3. The varactor circuit is tuned differentially to avoid common-mode noise from voltage supplies and other sources being up-converted close to the carrier and thus improves spectrum purity.

A differential transimpedance amplifier (M5–M6) is added to separate the common-source node of the oscillator, thereby preserving the second order harmonic which corresponds to a division ratio of 3. The input injection signal is AC-coupled to transistors M5–M6 and, after conversion into differential currents, mixed with the oscillator transistors M1–M4 and hence locked to the desired harmonic.

The first injection enhancement technique involves the introduction of inductor L_0 between the drains of M5 and M6. This inductor resonates with the parasitic capacitance at the input injection frequency and reduces the signal loss between external and internal injection points. There is a silicon-area penalty to be paid for this extra inductor. However, it is not substantial as the inductance required is small due to high input frequency of 60 GHz. The second harmonic enhancement technique is by introducing a feedback resistor R_f between the ILFD output and input. This resistor serves two purposes. Firstly, the DC voltage at the gate of M5 (or M6) is defined by the output DC voltage and the feedback resistance which yields a stable operating point for injection locking and no external DC biasing is required. This results in improved supply rejection and robust operation. The second and more important advantage of using the feedback resistor, is the improvement in injection efficiency of the ILFD. This is similar to [81], where resistive feedback is used to enhance the locking range of a 6 GHz ring oscillator based ILFD. In this work a similar technique is investigated for an LC-tank based ILFD. As L0 resonates at the third harmonic of output frequency, it generates an AC ground at the node. Thus the analysis can be carried out using half circuits. To this end, the output signal V_{out^+} can be given by

$$V_{out+} = V_{DC} + V_0 \cos(\omega_0 t + \theta) \tag{4.23}$$

where V_{DC}, V_0, ω_0 and θ is the DC voltage, amplitude, oscillator free-running frequency and phase of the output signal, respectively. The input voltage V_{in}, on the other hand, is the sum of the injection voltage V_{inj} and the feedback voltage and can be expressed as

$$V_{in+} = V_{DC} + \alpha V_0 \cos(\omega_0 t + \theta) + V_{inj+} \cos(\omega_{inj} t + \varphi) \tag{4.24}$$

where α is the feedback factor from output to input and V_{inj^+}, ω_{inj} and φ are the amplitude, frequency and phase of the input injection signal, respectively.

If the non-linearity higher than third order is ignored, the current I_+ of M1 is given by

$$\begin{aligned} I_+ &= a_0 + a_1 V_{in+} + a_2 V_{in+}^2 + a_3 V_{in+}^3 \\ &= a_0 + a_1\left[\left(V_{DC} + \alpha V_0 \cos(\omega_0 t + \theta) + V_{inj+}\cos(\omega_{inj} t + \varphi)\right)\right] \\ &\quad + a_2\left[\left(V_{DC} + \alpha V_0 \cos(\omega_0 t + \theta) + V_{inj+}\cos(\omega_{inj} t + \varphi)\right)\right]^2 \\ &\quad + a_3\left[\left(V_{DC} + \alpha V_0 \cos(\omega_0 t + \theta) + V_{inj+}\cos(\omega_{inj} t + \varphi)\right)\right]^3 \end{aligned} \tag{4.25}$$

The power of injection signal $\omega_{inj}(= 3\omega_0)$ can be obtained from the components of the above polynomial as

$$\begin{aligned} &a_1 V_{inj+}\cos(\omega_{inj} t + \varphi) + 3a_3 V_{DC}^2 V_{inj+}\cos(\omega_{inj} t + \varphi) \\ &\quad + a_3[\alpha^3 V_0^3 \cos^3(\omega_0 t + \theta)] \end{aligned} \tag{4.26}$$

Expanding the last term in (4.26) we get:

$$a_3[\alpha^3 V_0^3 \cos^3(\omega_0 t + \theta)] = \frac{a_3}{4}\alpha^3 V_0^3[\cos(3\omega_0 t + 3\theta) + 3\cos(\omega_0 t + \theta)] \tag{4.27}$$

The third harmonic $3\omega_0$ in the above equation which is fed-back from the output to the input, will enhance the injection if the first component of (4.27) is in phase with the injection signal V_{inj}. In other words, $(a_3 \cdot \alpha^3)/4 > 0$. In this conditional expression, a_3 is the small signal parameter g_m'' of the transistor M1.[1] A typical g_m'' of a MOS transistor is shown in Fig. 4.30. As the ILFD works at a range where $V_{gs} > V_{th}$, the g_m'' in this region is negative. The second parameter α is also negative as the input signal passes one common-source and one common-gate stage. Thus, the overall term $(a_3 \cdot \alpha^3)/4$ is positive and the feedback signal through the resistor R_f adds to the input injection signal and enhances the injection efficiency.

Unlike the circuit in [83] where the resistor is added serially to the tank to reduce the quality factor, the resistor in this design is in parallel with the LC tank. Therefore, the quality factor remains unaffected. Multiple oscillation modes are also damped by the resistive feedback by proper sizing of the resistors. The optimum value of the resistor is obtained by parametric simulations to achieve the required performance based on locking range, phase noise and injected power. The value of 3 kΩ, which is very large as compared to the effective resistance of the tank, keeps phase noise of the ILFD unaffected. The simulated phase noise of the ILFD during self-oscillation (with and without feedback resistor) is shown in Fig. 4.31.

[1]The drain current of a MOSFET can be written as a power series with respect to the gate-source voltage, i.e. $i_d(v_{gs}) = a_1 v_{gs} + a_2 v_{gs}^2 + a_3 v_{gs}^3 + \cdots$, where a_3 is the second-derivative (g_m'') of its transconductance [82].

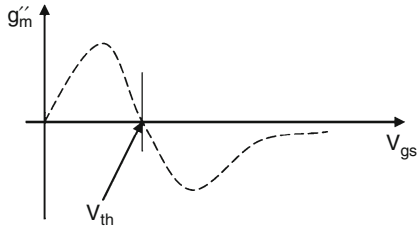

Fig. 4.30 A typical g_m'' of MOS transistor

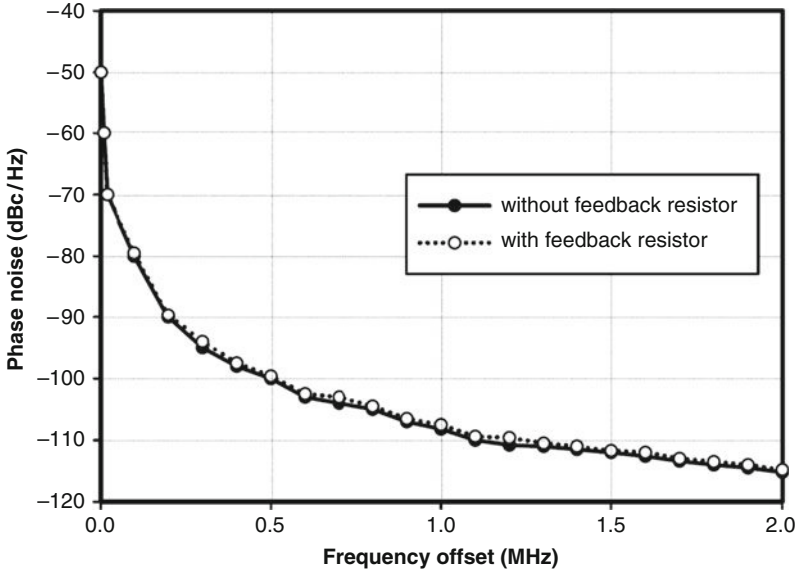

Fig. 4.31 Phase noise of the 60 GHz ILFD during self-oscillation, with and without feedback resistor

The IFLD was designed and fabricated in TSMC 65 nm bulk CMOS process. The PMOS transistors (M3–M4) are twice the NMOS transistors (M1–M2) to compensate their low mobility. The divider is designed for low voltage operation and supply voltage used in 0.9V. The total tank inductance is 245 pH and is composed of two inductors in series with each other. This approach reduces the length of output transmission lines and saves silicon area. Each inductor is a single turn 15 μm wide top-metal coil with a Q-factor of ∼28 at 20 GHz. The inductance and Q-factor of L_0, on the other hand, is 250 pH and 14 at 60 GHz. The tank capacitance is a combination of A-MOS varactors and fixed MIM capacitors and provide a capacitance tuning from 80 to 35 fF around 20 GHz (differential V_{tune} of 0–1.2). The corresponding Q-factor of the complete tuning circuit is between 11 and 17. The feedback resistor R_f is a polysilicon based RF resistor and has a very small silicon area in this technology. The core circuit has a small footprint of about

300 × 300 μm^2. The input and output signals are delivered by 50 Ω on-chip transmission lines and EM simulations are carried out to ensure proper impedance matching. The TLs are similar as the ones used for the 40 GHz ILFD. The divider is also measured by on-wafer probing using a similar setup as shown in Fig. 4.24b with the difference that the 60 GHz input signal is provided by an Agilent network analyzer (E8361) instead of a signal generator. The input 60 GHz signal is applied to a wave-guide based single-to-differential converter and then passed on the RF probe using semi-rigid probes to avoid mismatch between differential inputs. The output differential signal is converted to single-ended using a low frequency hybrid and applied to the spectrum analyzer (SA). The die micrograph is shown in Fig. 4.32 and occupies 800 × 500 μm^2 including the output buffers, transmission lines, and pads.

The free-running oscillation frequency of the ILFD is first measured in the absence of injection signal. The measured value of 16.5–18.1 GHz is about 2.7 GHz lower than the expected free-running frequency of 19–21 GHz. The cause of this considerable shift is analyzed by going back to the schematic and the layout of the circuit. It is noted that the interconnect inductance between the two tank inductors was underestimated which resulted in an unaccounted inductance of ∼80 pH. Adding this inductance to the original simulations, results in a simulated free-running frequency range matching the measured range. The operation of the divider however, can be verified by injecting a frequency, which was approximately three times the actual measured free running frequency.

The sensitivity of the divide-by-3 ILFD is measured for a number of differential tuning voltages (V_{diff}). For each voltage, minimum input power is determined for which the divider still locks to the input frequency. The ILFD can operate from 48.8 to 54.6 GHz (∼6 GHz or 11.2% locking range) with a maximum injected power of +2 dBm. The input power between −55 and −60 dBm close to free running frequency of ILFD is very low due to the harmonic enhancement technique applied in this design. The measured input sensitivity versus frequency, after de-embedding losses is shown in Fig. 4.33. The locking range for one tuning voltage lies between 1 and 2 GHz. The divider operates with a 0.9 V supply and draws a current of 3.3 mA. The screen-shots of locked frequency spectrums for maximum and minimum

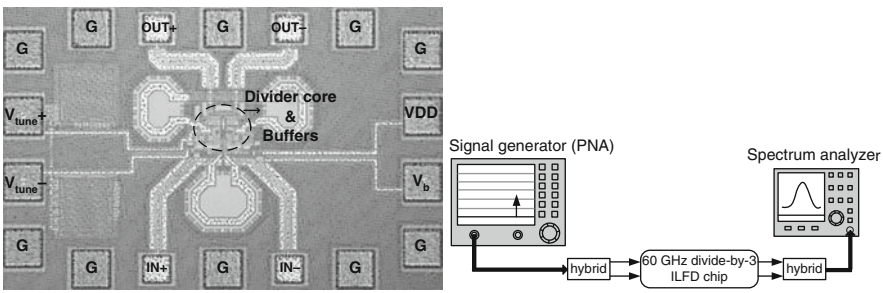

Fig. 4.32 Sixty gigahertz divide-by-3 ILFD chip micrograph and measurement setup

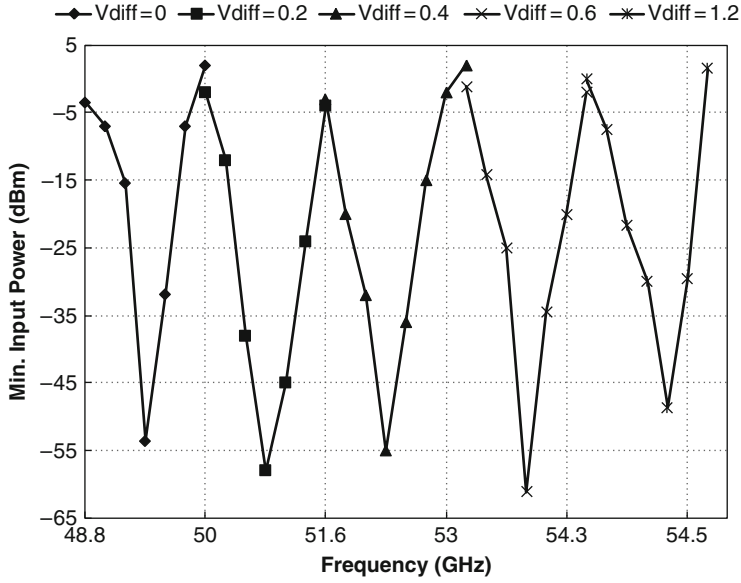

Fig. 4.33 Measured input sensitivity of the 60 GHz divide-by-3 ILFD

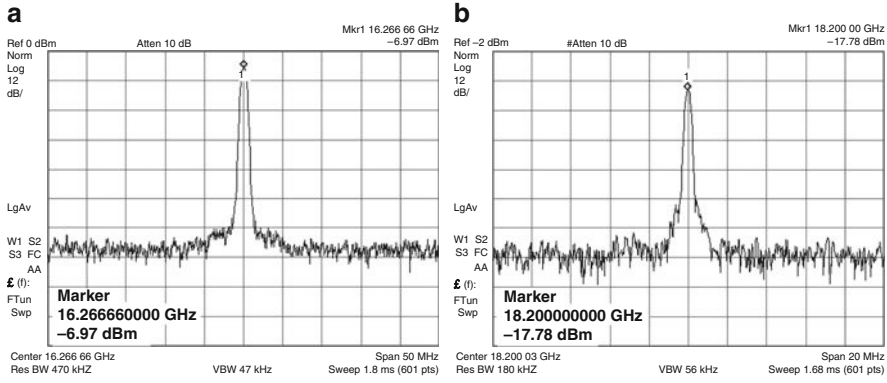

Fig. 4.34 Sixty gigahertz ILFD screen-shots: minimum frequency (**a**), and maximum frequency (**b**)

operation frequencies are shown in Fig. 4.34. The output power of the divider, after subtracting the losses of the measurement set-up, lies between −1 and −5 dBm over the complete operating range. The measured output power level is sufficient to drive the next divider stages. The phase noise of the ILFD is −115 dBc/Hz at 1 MHz for a 18.2 GHz divided output frequency. The phase noise of the input signal generator at three times the frequency is −105.2 dBc/Hz which is slightly higher than the theoretical 9.5 dB difference due to frequency division. The phase noise variation over the operation range is ±3 dB but it is still within the target

specification of <-100 dBc/Hz at 1 MHz offset. The phase noise plot at the highest end of the locking range for an input frequency of 54.6 GHz (corresponding to 18.2 GHz divided output) is shown in Fig. 4.35.

4.1.5 Monolithic Transformer Design and Measurement

This section presents the design and measurement of a monolithic transformer which is utilized in the dual-mode ILFD (Section 4.1.6) and the transformer coupled VCO (Section 4.2.5). The transformer structures commonly used are based on multi-turn interleaved or stacked interleaved coils. These structures are suitable to realize large inductance values in the nano-henry range. However, as the required inductance in the above mentioned designs is around 70 pH, a smaller and simpler structure is introduced which is based on a single-turn stacked structure. Occupying a small silicon foot-print, it is suitable to realize low inductance values with medium to high coupling factor (between 0.5 and 0.8).

The transformer is implemented with an octagonal single turn primary coil in Me6 and a similar coil in Me5. The top metal (Me6) in the available technology is 3.4 μm thick and yields a high Q-factor owing to lower loss. Me5 layer is exactly placed below the primary coil to increase coupling. As shown in Fig. 4.37a, the long vertical terminals commonly used for connections are not included; rather the space between the ports is just kept large enough to fit-in the varactors. This approach greatly helps to ease routing and also decreases the interconnect parasitics. Me1 is placed under the transformer to provide isolation and reduce capacitive coupling to the substrate. The transformer is simulated in ADS Momentum using a custom-made model of the technology stack. The simulated parameters of the transformer are shown in Fig. 4.36. At 60 GHz, the inductance of the primary and secondary

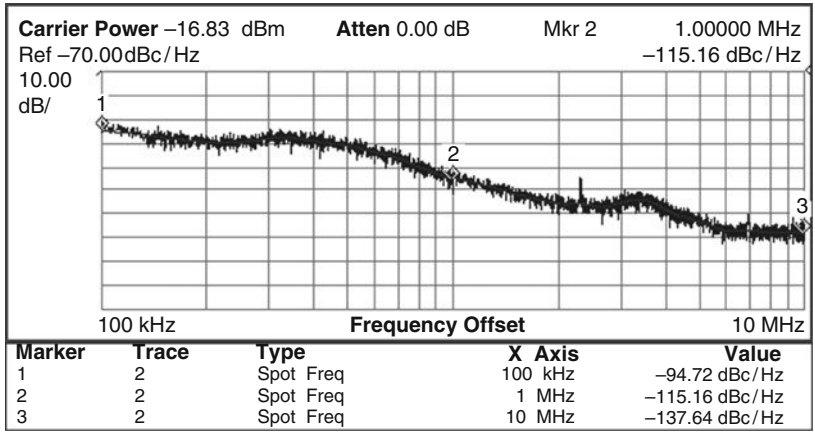

Fig. 4.35 Sixty gigahertz divide-by-3 ILFD phase noise at 18.2 GHz locked output

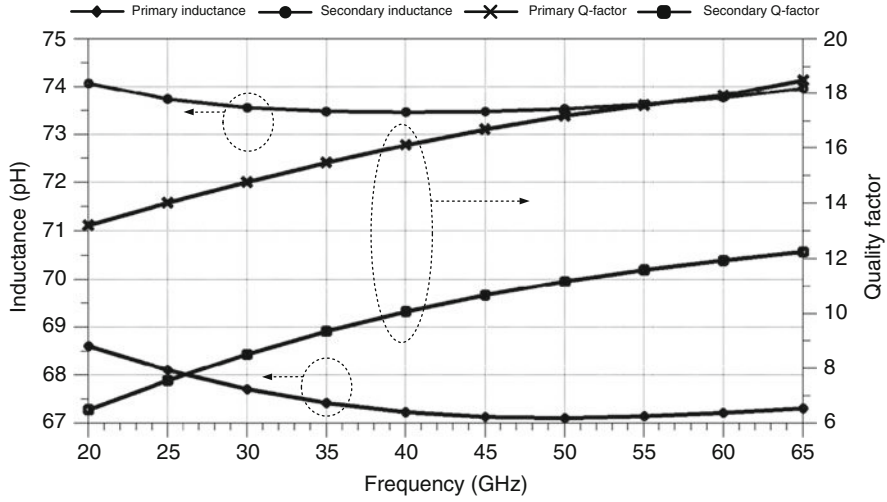

Fig. 4.36 Simulated inductance and Q-factor of primary and secondary coils of the transformer

coils is 67 pH and 74 pH with a Q-factor of 18 and 12, respectively. The coupling factor, calculated using H-parameters is 0.76.

The transformer is fabricated as a separate test-structure to validate the values obtained from EM simulations. The low value of the inductance, which is of the same order as interconnect inductance necessitates the need of de-embedding structures. These structures cancel-out the effect of bond-pads as well as interconnect path connecting the bond-pads to the transformer. In other words, the measurement plane is shifted exactly at the terminals of the transformer. Open, short and load de-embedding structures are utilized in this design to characterize the transformer up to 65 GHz. The chip micrograph of the transformer and de-embedding structures is shown in Fig. 4.37b. The transformer only occupies $54 \times 52\ \mu m^2$ and it can be seen that its dimensions are smaller than a "ground" bond-pad.

The transformer is measured using Agilent E8361 PNA and Cascade Microtech's WinCal XE calibration tools. Impedance standard substrate (ISS) is first used to calibrate the measurement system so that the measurement plane is at the probe-tips. After an acceptable calibration (below 1% variation), the s-parameters of the transformer as well as the de-embedding structures are measured. The measurements were repeated and subsequently averaged, after confirming the calibration validity each time. The s-parameters are then post-processed in ADS to de-embed the contribution of bond-pads and interconnect paths. The resulting measured inductance is presented in Fig. 4.38. The primary coil demonstrates an inductance of 70 pH whereas the secondary coil has an inductance of 88 pH at 60 GHz. The measured coupling factor at 60 GHz is 0.69 as shown in Fig. 4.39. The simulated 'k' is also shown for comparison. The satisfactory results of the transformer enabled its utilization in the TC I-Q VCO in Section 4.2.5 and in the dual-mode frequency divider in Section 4.1.6.

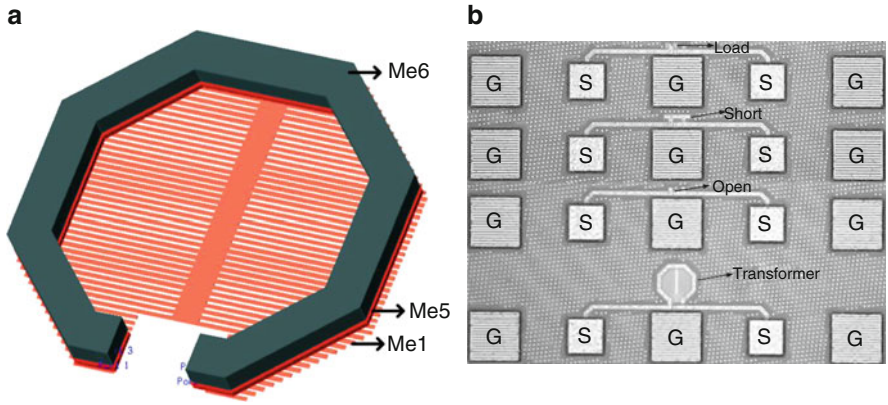

Fig. 4.37 Transformer structure (**a**) and chip micrograph of transformer and de-embedding structures (**b**)

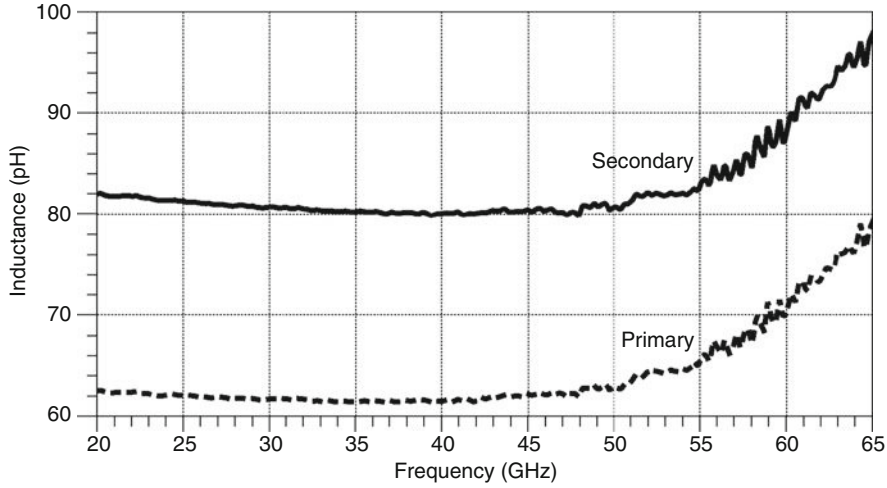

Fig. 4.38 Measured inductance of primary and secondary coils of the transformer

4.1.6 Dual-Mode (Divide-by-2 and Divide-by-3) ILFD

The preceding two sections have presented two ILFD circuits able to divide-by-2 and divide-by-3, respectively. The 40 GHz ILFD based on direct injection satisfies the specification of locking range with some margin, whereas the 60 GHz ILFD based on resistive harmonic enhancement, though demonstrating sufficient locking range, is off-target with respect to operation frequency. This section is dedicated to investigation and design of a dual-mode prescaler which could replace the two independent dividers and offer both divide-by-2 and divide-by-3 operation. This

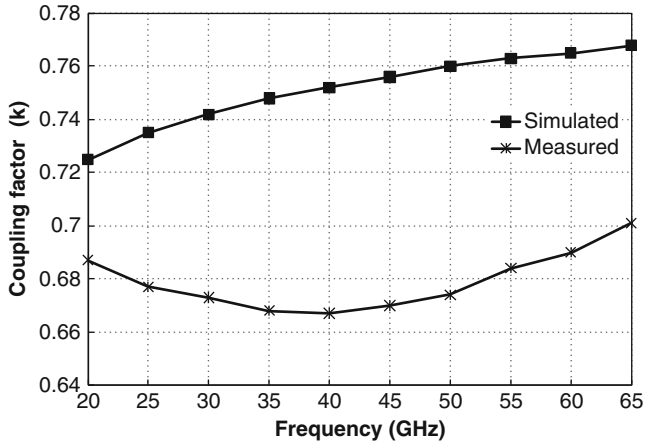

Fig. 4.39 Simulated and measured coupling factor of the transformer

approach offers a number of advantages. Firstly, it simplifies the overall design as it alleviates the need of switchable prescalers for the flexible synthesizer. Secondly, it reduces the power consumption of the overall circuit and lastly, considerable saving in silicon area is possible by reducing the number of prescalers from two to one.

The conventional divide-by-2 topology with tail injection [66] cannot be used for divide-by-3 as even-order non-linearity is not preserved. Similarly, the divide-by-3 ILFD presented in the preceding section is not able to operate in divide-by-2 mode as mixing of a differential input signal with harmonics due to odd-order non-linearity only generates common-mode signal and the differential-mode signal is cancelled out. Therefore, a change in injection topology which could preserve both even and odd-order non-linearity and generate differential-mode output signal is required.

A solution proposed recently in [84] involves two separate injection points for divide-by-2 and divide-by-3 operation. The former is achieved by using the conventional topology of tail injection and the latter is accomplished by introducing an extra coil in the vicinity of the tank inductor forming a balun. This converts the single-ended input injection signal (around three times the self-oscillation frequency of the tank) to a differential-mode signal and mixes it with the cross-coupled pair to generate the desired divided-by-3 output. The down-side of this solution is the requirement of two separate injection ports and possible leakage of output signal to the injection port through the balun in the divide-by-3 mode.

In this book, two ILFD circuits are presented which, based on the input frequency are able to divide-by-2 or 3. The two variants are shown in Fig. 4.40. In these circuits, both the odd and even order non-linearity of the cross-coupled pair are preserved generating their respective harmonics. In Fig. 4.40a, two NMOS transistors M3–M4 are utilized as injection transistors where as in Fig. 4.40b, an

NMOS transistor M3 and a PMOS transistor M4 are used for the same purpose. The strength of harmonics decreases as the order increases and the most dominant ones are the second and third harmonic. In order to increase the non-linearity, which would enhance the harmonic strength, the mixer (cross-coupled pair) needs to be driven with large signals. To this end, transformer feedback is utilized to increase the effective drain-source voltage of M3 and M4 in both circuits. The coupling between the primary and secondary of the transformer is done in a way to cancel the

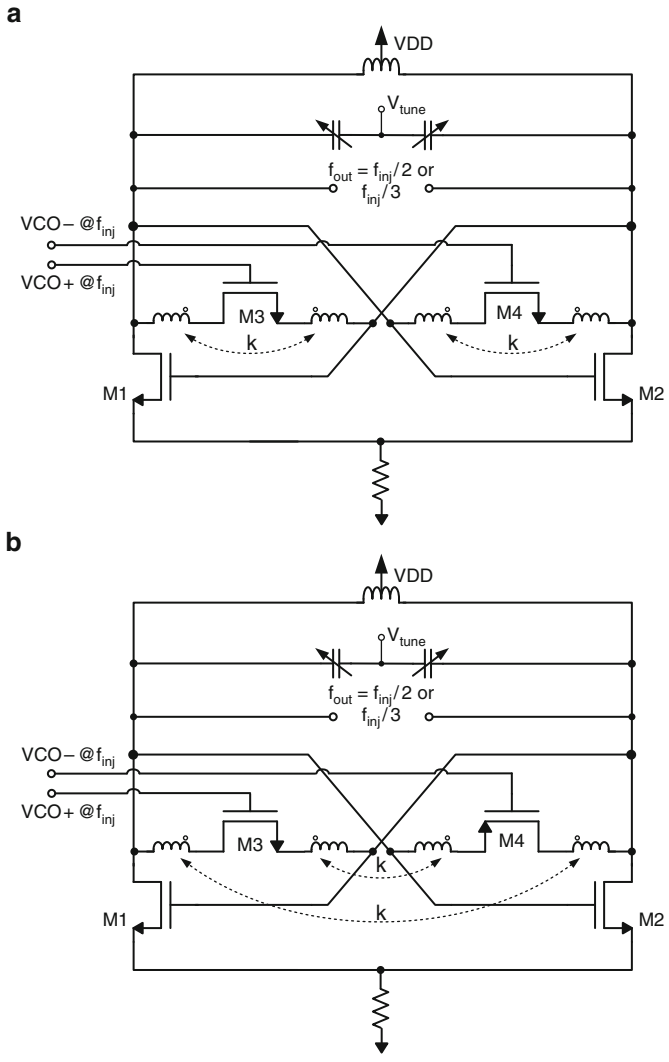

Fig. 4.40 Dual-mode ILFD able to divide-by-2 and 3; NMOS-NMOS injection (**a**), and NMOS-PMOS injection (**b**)

miller capacitance [85] of the injection transistors and to achieve symmetric injection for the differential input. The use of transformer feedback also increases the over-drive voltages of the injection transistors resulting in enhancement of their effective transconductance. The signal mixing between the injection signal and the tank oscillation frequency is carried out between the gate and drain of M1 and M2 and due to higher injection efficiency, wider locking range is achieved. A variant of this approach using series-peaking only was presented in [86] for a divide-by-2 ILFD and single-ended injection. Both circuits have been simulated in Cadence™ and optimized for wide locking range covering the required frequency bands at 40 GHz for divide-by-2 and 60 GHz for divide-by-3 operation. However, due to limited availability of silicon area, only the NMOS-NMOS injection variant in Fig. 4.40a is selected for IC implementation and will be referred to as the dual-mode ILFD, hereafter.

The LC-tank of the above ILFD is formed by a center-tap inductor, a varactor setup and parasitic capacitance of transistors. The center-tap inductor is a 9 μm wide single-turn top-metal coil having an inductance of 192 pH and Q-factor of ∼28 around 20 GHz. The varactors provide a capacitance tuning of 150–39 fF with a Q-factor 8–20, for a tuning voltage of 0–1.2 V, respectively. Due to only-NMOS cross-coupled structure, the circuit can operate with low supply voltages and is designed for a 0.8 V operation. The dimensions of the injection transistors are determined in combination with the required inductance in their source and drain terminals. The external RF-input is AC coupled and the biasing is achieved using a resistive voltage divider on-chip. Detailed AC and transient simulations over the complete locking range are done to extract optimized inductance and coupling values for the transformer. Differential common-source output buffers are employed for measurement purposes and matched to a 50 Ω environment.

The basic aim of the transformer is to enable transistors M3 and M4 to transfer the input injection signal at 40 or 60 GHz without loss for signal-mixing. The transformer presented in Section 4.1.5 is utilized in this design. Recalling, the primary and secondary coils of the transformer have a measured inductance of 70 and 88 pH at 60 GHz and 62 and 80 pH at 40 GHz. The coupling factor at the two frequencies is 0.67 and 0.69, respectively.

The dual-mode ILFD is designed and fabricated in TSMC C65nm process and the chip micrograph is shown in Fig. 4.41. The input and output coplanar transmission lines are characterized along with the bond-pads and are wide-band 50 Ω matched. The signal and ground plane is 2 and 10 μm wide and the spacing between them is 6 μm. The core circuit occupies 200 × 150 μm^2 only whereas the total chip area is 800 × 500 μm^2. The measurement setup is similar to the one used for the 60 GHz divide-by-3 ILFD in the preceding section. The input signal for both frequency bands at 40 and 60 GHz are provided by an Agilent network analyzer (E8361) and the output spectrum and phase noise are measured with a spectrum analyzer.

The free-running oscillation frequency in the absence of an injection signal is between 16.8 and 19.2 GHz for a varactor tuning voltage of 0–1.2 V. For a supply voltage of 0.8 V, the current and power consumption of the ILFD is 5 mA and 4

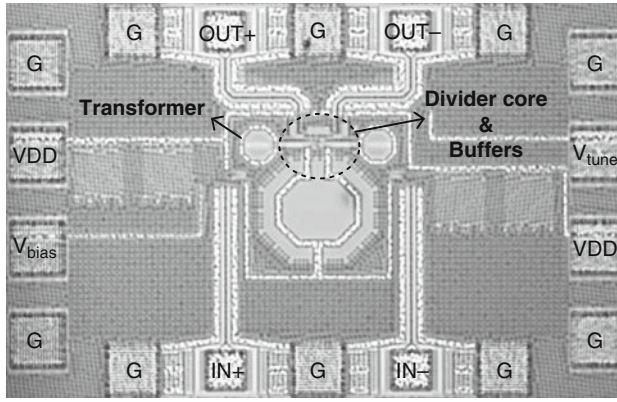

Fig. 4.41 Dual-mode (divide-by-2 and 3) ILFD micrograph

mW, respectively. The divide-by-2 operation of the ILFD is verified by injecting a signal close to double of the free-running frequency. The input power is then decreased and the minimum power required to lock to the injection frequency is noted. By sweeping the input frequency the locking range is determined for a particular varactor tuning voltage. The process is repeated for V_{tune} between 0 and 1.2 V. The resulting sensitivity curves are shown in Fig. 4.42. The input power required is lower than −2 dBm. The locking range for each tuning voltage is about 3 GHz (8.3%) and the total operation range in divide-by-2 mode is from 33 to 39.5 GHz (17.9%). An example of locking operation in divide-by-2 mode can be seen in Fig. 4.43a. The unlocked ILFD is free-running at 18.475 GHz for V_{tune} of 0.65 V. When a signal at 36.956 GHz is injected, the ILFD locks to exactly half of this frequency (18.478 GHz). The unlocked signal demonstrates relatively high phase noise as shown by the finite slope. On the other hand, once locked to the injection signal, the output signal becomes well defined and the phase noise is also reduced. The divide-by-3 operation of the ILFD is confirmed by injecting a signal at 58.755 GHz which is close to three times of the free-running frequency. The resulting sensitivity curves are also shown in Fig. 4.42. The maximum required input power of +1 dBm is slightly higher than divide-by-2 mode as the third harmonic is relatively weaker than the second harmonic. The average locking range for each tuning voltage is about 4 GHz (7.4% locking range) and the total operation range in divide-by-3 mode is from 48.5 to 59.5 GHz (20.4% operating range). Figure 4.43b shows the locking operation in the divide-by-3 mode and the improvement of spectrum purity and phase noise is visible as in the divide-by-2 mode. A shift in the free-running frequency is observed between simulations and measurements and is potentially caused by interconnect parasitics. Re-simulating after adding ∼50 fF capacitance in the LC-tank results in a close match to the measured free-running frequency. The above discrepancy can be corrected in a re-run by lowering the tank inductance accordingly. Barring the shift in frequency, the

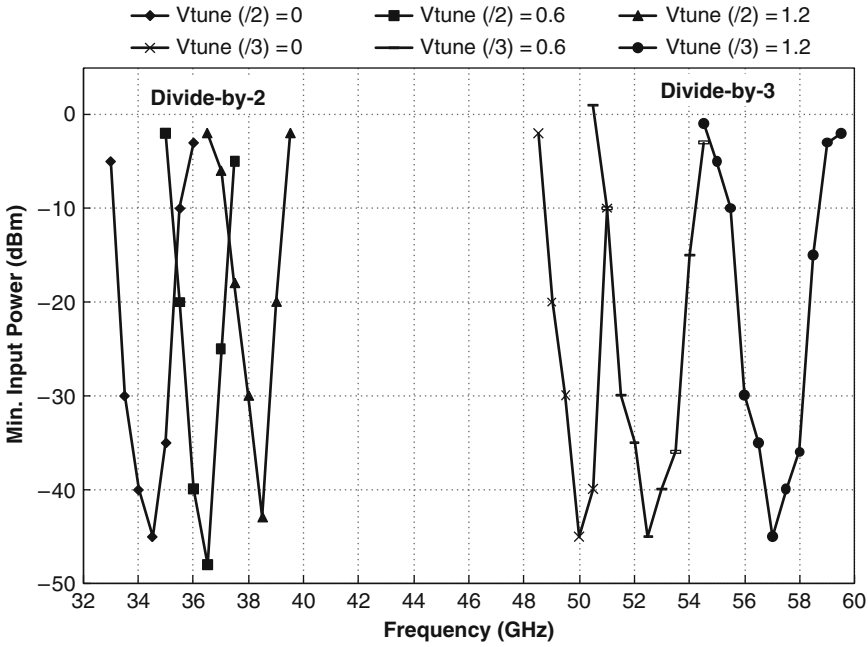

Fig. 4.42 Measured input sensitivity of the dual-mode ILFD

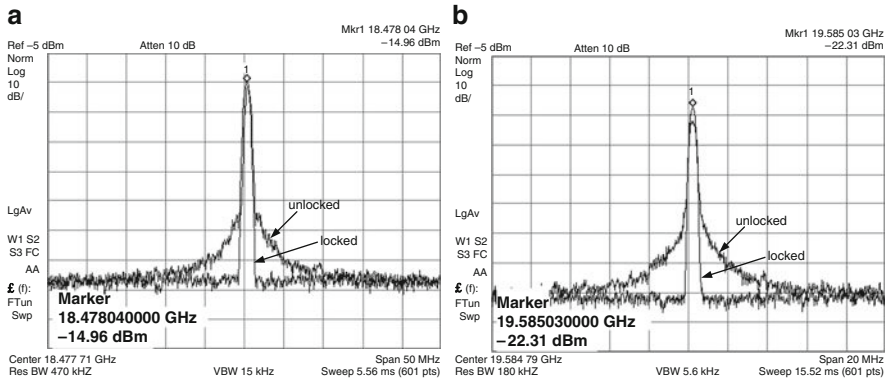

Fig. 4.43 Locked and unlocked spectrum screen shots: divide-by-2 mode for an input frequency of 36.956 GHz (**a**), and divide-by-3 mode for an input frequency of 58.755 GHz (**b**)

11 GHz operation range can easily cover the required 57–63.6 GHz band for the 60 GHz synthesizer.

The output power of the ILFD is also measured over the complete operation range and cable and other measurement losses are de-embedded from it. A maximum

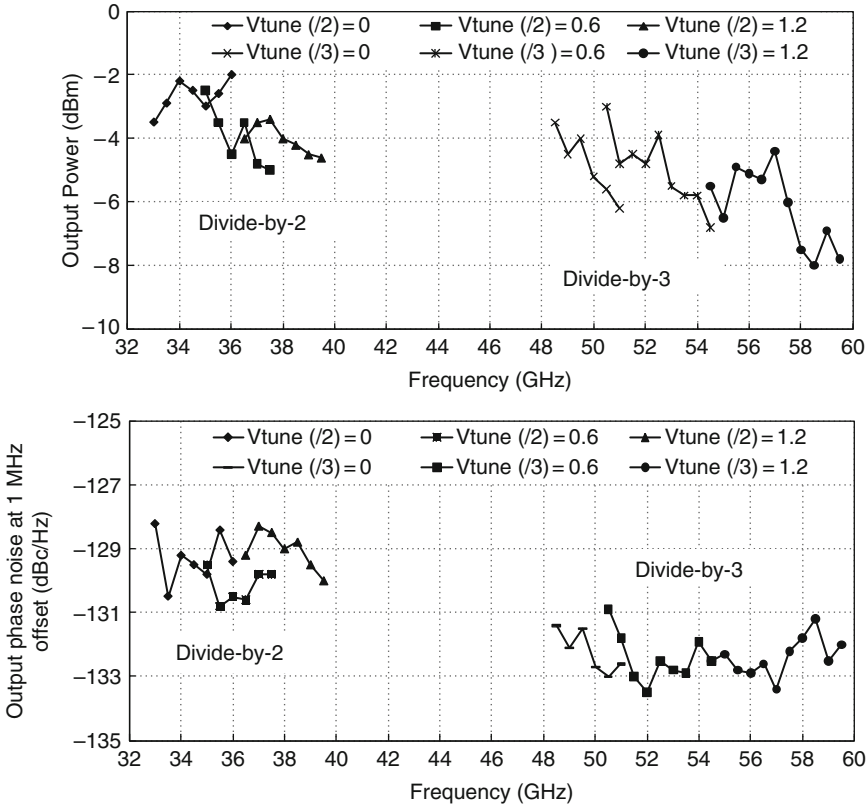

Fig. 4.44 Output power (*top*), and phase noise (*bottom*) variation of the dual-mode ILFD over the operation range

variation of ±3 dB in the output power level is observed for the two division modes as shown in Fig. 4.44. The output power is high enough to drive the next divider stages in the synthesizer feedback loop. The phase noise is also measured in both modes of division and demonstrates a maximum ±1.15 dB variation over the complete operation range of both modes (see Fig. 4.44). The measured values satisfy the phase noise specifications of the prescaler. Two such measurements of the locked ILFD are shown in Fig. 4.45. In the divide-by-2 mode, the phase noise at the locked output of 19.05 GHz (input frequency of 38.1 GHz) is −130.6 dBc/Hz at 1 MHz offset. On the other hand, in the divide-by-3 mode, phase noise is −132 dBc/Hz for a divided output of 16.6 GHz (input frequency of 49.8 GHz). The generator phase noise at 1 MHz offset is −124.8 dBc/Hz during divide-by-2 injection and −123 dBc/Hz for divide-by-3 injection. The output phase noise values are approximately equal to the theoretical 6 and 9.5 dB phase noise improvement due to frequency division by 2 and 3, respectively.

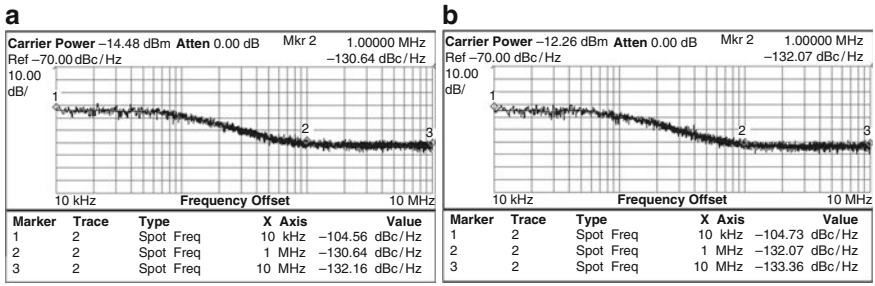

Fig. 4.45 Phase noise of a locked ILFD: divide-by-2 mode (**a**), and divide-by-3 mode (**b**)

4.1.7 ILFD figure-of-Merit (FOM)

Injection locked frequency dividers are usually compared based on their individual performance parameters such as operation frequency, locking range, input power and DC power consumption. Keeping in mind the inherent narrow-band nature of ILFDs, the most important parameter from the above list is indeed the locking range. Ideally, the complete locking range should be covered without any tuning; however, in practice the locking range for each tuning voltage is limited, necessitating the need for varactor tuning. It is observed in literature that the locking range parameter is interchangeably used for frequency ranges obtained with [87] or without [83] employing any varactor tuning. Therefore, for a fair comparison between ILFDs which do and do-not require varactor tuning, a figure-of-merit incorporating this difference is required.

In order to achieve the above-mentioned FOM, let us consider a typical input sensitivity curve of an ILFD. Shown in Fig. 4.46, the total locking range of the ILFD can be divided into 'p' smaller ranges denoted by $f_1, f_2, \ldots, f_p$ each due to a specific tuning voltage $V_{tune\text{-}1}, V_{tune\text{-}2}, \ldots, V_{tune\text{-}p}$, respectively. Each curve also has its minimum input power $P_{min\text{-}1}, P_{min\text{-}2}, \ldots, P_{min\text{-}p}$.

These smaller ranges may or may not be equal in width, so an average range can be defined as

$$f_{avg} = \frac{f_1 + f_2 + \cdots + f_p}{p} = \frac{1}{p}\sum_{i=1}^{p} f_i \tag{4.28}$$

To include the effect of varactor tuning, we define a variable 'n', such that n times the average locking range is equal to the complete locking range of the ILFD, i.e.

$$f_{\max} - f_{\min} = f_{lock} = n \cdot f_{avg} \tag{4.29}$$

The variable 'n' can be understood with an example. A value of $n = 1$ means that ILFD covers the complete frequency range without varactor tuning whereas $n = 5$

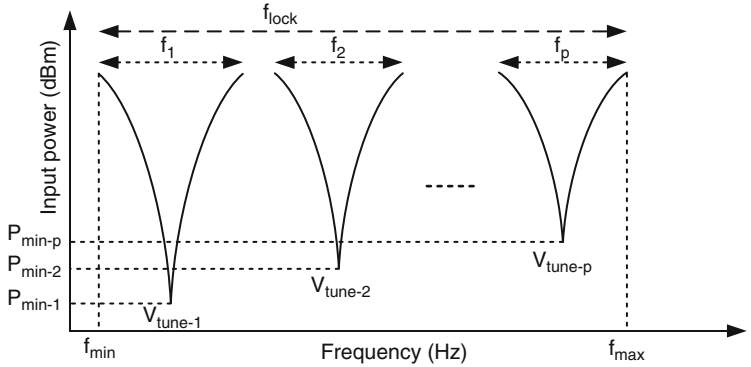

Fig. 4.46 Typical input sensitivity of an ILFD

implies the requirement of five smaller locking ranges to cover the same frequency range. Clearly, a smaller value of 'n' is preferred.

ILFDs require a certain power to successfully lock to the input signal. The smaller this required input power the better the ILFD. This power may differ for every 'p' frequency curve as shown in Fig. 4.46. Similar to the frequency average in (4.28), an average minimum power can also be defined and denoted as $P_{min-avg}$. Resultantly, the first FOM can now be defined as

$$FOM_{P_{in}} = 10\log\left(\frac{1\,mW}{P_{\min-\text{avg}}}\cdot\frac{f_{lock}}{n\cdot f_{center}}\right) \tag{4.30}$$

where the subscript 'P_{in}' refers to the FOM reflecting the injection efficiency by assessing the average injection power $P_{min\text{-}avg}$ required for an average relative tuning range (f_{avg}/f_{center}). The FOM is defined in a way that a higher FOM_{Pin} indicates a better ILFD.

Power consumption is another performance benchmark regularly used for ILFDs. On the same lines as FOM_{Pin}, a second figure-of-merit FOM_{Pdc} is defined which reflects the tuning efficiency by assessing the DC power consumption needed for an average relative tuning range and is written as

$$FOM_{P_{dc}} = 10\log\left(\frac{1\,mW}{P_{dc}}\cdot\frac{f_{lock}}{n\cdot f_{center}}\right) \tag{4.31}$$

where the subscript 'P_{dc}' refers to the FOM based on DC power consumption and P_{dc} is the power consumption in watts. Similar to the first FOM, a more positive value of FOM_{Pdc} indicates a better ILFD.

Table 4.2 summarizes the performance of the presented dividers in the preceding sections and includes the proposed FOM for all designs. Furthermore, a divide-by-2 ILFD presented in [88] is included for reference. If compared to the ILFD of Section 4.1.3, the sensitivity of the latter is better than the cited reference with

Table 4.2 FOM for the presented frequency dividers and [88] for comparison

Reference	f_{lock} (GHz)	LR (%)	n	$P_{min\text{-}avg}$ (dBm)	P_{dc} (mW)	FOM_{Pin} (dB)	FOM_{Pdc} (dB)
Section 4.1.2 (Divide-by-2 SFD)	2–35.5	178.6	1.0	−20.1	28.8	52.6	17.9
Section 4.1.3 (Divide-by-2 ILFD)	30.3–44.0	37.0	2.2	−36.3	9.0	58.5	12.7
Section 4.1.4 (Divide-by-3 ILFD)	48.8–54.6	11.2	5.0	−55.2	3.0	68.7	8.7
Section 4.1.6 (Dual-mode ILFD)	÷2 33–39.5	17.9	2.3	−45.3	4.0	64.2	12.9
	÷3 48.5–59.5	20.4	2.8	−45.0		63.5	12.5
[88] (Divide-by-2 ILFD)	35.7–54.9	42.3	1.0	−26.0	0.8	52.2	27.2

comparable locking range, thus its FOM_{Pin} is better. On the other hand the ILFD in [88] consumes 0.8 mW as compared to 9 mW by the one in Section 4.1.3. Thus FOM_{Pdc} of the latter is lower which is expected as it offers quadrature outputs as opposed to non-quadrature operation of the cited reference. It should also be noted, that the ILFD of [88] does not employ varactor tuning, thus its 'n' is equal to 1, whereas it is 2.22 for the ILFD of Section 4.1.3, implying the use of varactors.

4.1.8 Summary

Section 4.1 has presented a number of prescaler architectures as potential components for the proposed synthesizer. Beginning with an overview of prescalers, a static frequency divider was presented in Section 4.1.2. Although it demonstrates broadband operation, it is unable to reach the 40 GHz target frequency. On the other hand, the 40 GHz divide-by-2 ILFD presented in Section 4.1.3 based on direct injection, covers the desired frequency band with some margin. The 60 GHz divide-by-3 ILFD in Section 4.1.4 demonstrates improved locking range thanks to resistive harmonic enhancement. However, it has a considerable frequency shift due to layout inaccuracy. The last divider architecture presented is a dual-mode ILFD able to divide by 2 and 3; it demonstrates adequate locking range for both modes of operation. New figure-of-merits have also been introduced which incorporate the difference between ILFDs with and without varactor tuning along with the input sensitivity and DC power consumption bench-marks.

4.2 Voltage Controlled Oscillator

The voltage controlled oscillator (VCO) is the second component of the synthesizer front-end that is operating at the highest frequency. VCOs can be considered as the "heart" of the synthesizer as they provide the actual oscillation signal at the output

and define some of the most important performance parameters of the synthesizer. For instance, the tuning range of the VCO determines the range in which the PLL can lock or the synthesizer can generate output frequencies. Similarly, phase noise of the VCO dominates the overall synthesizer phase noise outside the loop bandwidth. The spectral purity of the synthesizer output is also dependent on the VCO implementation and its ability to reject common-mode noise being up-converted close to the carrier frequency. Another important contribution of the VCO is the power consumption in the overall power budget of the synthesizer. Therefore, it is evident that a decent VCO design can almost ensure a good synthesizer performance.

This section is dedicated to the VCOs designed and implemented for the proposed synthesizer. After providing a short overview of different VCO architectures, three VCOs targeting the 40 and 60 GHz front-ends are explained. In addition, the design and measurement of a monolithic transformer, utilized in a 60 GHz VCO is elaborated. Lastly, investigation into dual-band VCO architectures is presented.

4.2.1 Overview of VCO Architectures

The voltage controlled oscillator is one of the most researched and published integrated components in literature. Over the years, tens of different oscillator architectures have been reported. However, for this work, oscillators having the potential for mm-wave operation will be considered only. MM-wave VCOs can be divided into two main categories: resonator-less and resonator-based VCOs as shown in Fig. 4.47. Oscillators require complex poles to ensure oscillation. In case of resonator-less oscillators, which are implemented with capacitors or inductors (one type of reactive element only), resistance (of a resistor or a transconductor) and feedback are needed to make the resonator-less oscillator work. In other words, explicit feedback is necessary to create complex poles out of the real poles created by the reactive elements [89].

An example of such a resonator-less oscillator is the well known ring oscillator (Fig. 4.48a) which consists of a cascade of inverting gain stages with the output of

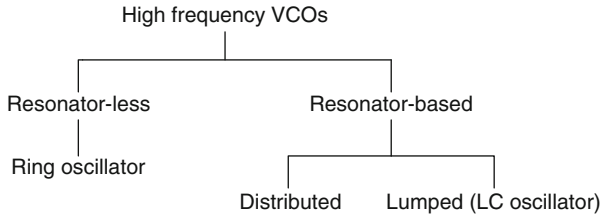

Fig. 4.47 Categorization of high frequency VCO architectures

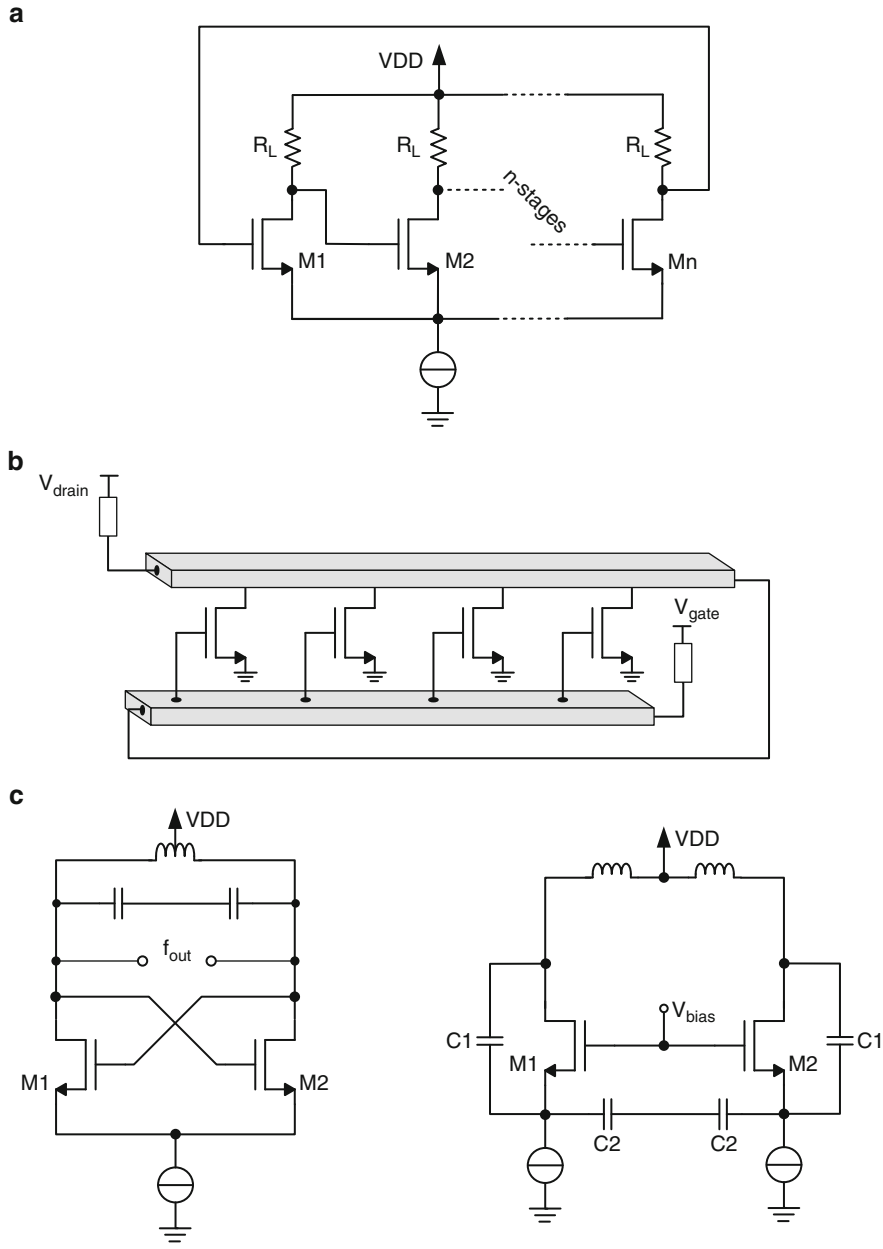

Fig. 4.48 Resonator-less VCO; ring oscillator (**a**). Resonator-based VCOs: distributed (**b**), LC-VCOs. negative-Gm (**c**, *left*), Colpitts (**c**, *right*)

the last inverter connected to the input of the first one in an inverted fashion. The frequency of oscillation depends on the number of inverter stages and the delay per stage. At the oscillation frequency, the phase through the ring oscillator is 360°, half of which is contributed by the feedback connection. The other half is equally distributed among the number of stages, i.e. $\Delta\Phi = 180°/N$, where N is the number of the stages and $\Delta\Phi$ is the phase shift introduced by one stage. For a two stage ring oscillator N equals 2 and the outputs are 90° out of phase with each other. The ease of available quadrature (or multi-phase) outputs is a considerable advantage of non-resonator based ring oscillators. In addition, they require small silicon-area due to absence of inductors and capacitors. The tuning of ring oscillators is usually achieved by varying the transconductance of the delay stages (by changing bias current) resulting in wide tuning range above 30%. The down-side of ring oscillator is the inferior spectral purity and phase noise performance. This is primarily because their effective Q-factor is close to unity and noise active and passive devices lie in the signal path [90]. Furthermore, the reported ring oscillators in Bulk CMOS processes are limited to 10∼15 GHz and one 31 GHz reported implementation in SOI CMOS [91] barely reaches the mm-wave regime. Due to these reasons ring oscillator based VCOs are not a popular choice for mm-wave frequency synthesizers.

The second category of high frequency VCOs are the resonator-based ones which are further divided into distributed or lumped, depending on the implementation of the resonator. A resonator (also called a tank circuit) inherently has complex poles, which are formed by inductors and capacitors (two types of reactive elements) in the lumped case and the same is true for the equivalent circuit of the distributed resonator. A conventional distributed VCO (DVCO) is shown in Fig. 4.48b and is formed by feeding the output of a distributed amplifier (also referred to as travelling-wave amplifier) back to its input. The DVCO consists of two transmission lines: the gate line and drain line, and transistors providing the gain. The forward (to the right in the figure) wave on the gate line is amplified by each transistor and the incident wave on the drain line travels in synchronization with the wave on the gate line. Each transistor adds power in phase to the signal. Terminations on the gate and drain line absorb the oppositely travelling waves on the corresponding lines. The oscillation frequency is determined by the round-trip time delay [92], i.e.

$$f_{osc} \approx \frac{v_{pv}}{2nl} \approx \frac{1}{2nl\sqrt{LC}} \tag{4.32}$$

where n is the number of transmission line segments each of length l. $v_{pv} = 1/\sqrt{LC}$ is the phase velocity of the waves in the transmission line and L and C are the inductance and capacitance per unit length of the transmission line including the transistor capacitances. The tuning in DVCOs is achieved either by adding varactors to transmission lines or changing the effective length which the signals have to traverse. The former approach has the down-side of introducing an extra

zero-bias capacitance to the line which does not contribute in tuning. An alternative is to utilize the parasitic capacitances of the transistors themselves, by changing the biasing voltage. However, this approach requires careful design to maintain a stable operating point for all biasing voltages. As an example, a 10 GHz CMOS DVCO in [92] demonstrates a tuning range of 9% by tuning the biasing voltage of transistors and 2.5% tuning range by varying the effective length of transmission lines.

There are a number of apparent advantages of DVCOs. Firstly, since distributed amplifiers can have a bandwidth close to f_{max} of a given technology, distributed oscillators, theoretically, can also operate at frequencies close to f_{max}. Secondly, with the proper choice of the number of transistors and their spacing, a DVCO can also generate quadrature or multi-phase signals. However, despite these advantages DVCOs have not been fully exploited due to a number of open issues. Firstly, the on-chip terminations, which are expected to absorb waves travelling opposite to the signal wave, have implementation and matching problems. As on-chip passives have a finite absolute tolerance, achieving an exact impedance value is highly likely to have mismatch. This leads to unwanted reflections from these terminations back into the oscillator, degrading the performance. Another major challenge in a DVCO is to synchronize the signals on the drain and gate transmission lines. Due to unequal admittances at the input and output of transistors, the phase velocity at the gate and drain is unlikely to be equal in real implementations. This may require compensation in one of the lines by adding passive structures which again pose the problem of inaccuracy on chip. The example in the preceding paragraph also points to the tuning range limitation for DVCOs at mm-wave frequencies. Due to the above-mentioned issues, DVCOs have yet to find a place as main stream VCO choice in mm-wave CMOS circuits.

The second type of resonator-based VCOs includes lumped passive components, i.e. inductors (L) and capacitors(C) and therefore termed as LC-VCOs. This type of VCOs has undoubtedly been the most popular choice for high frequencies due to their simple structure and reasonably-good phase noise performance. LC-VCOs can further be divided into two types: negative-Gm oscillator and Colpitts oscillator. The difference between the two is the method, by which the losses of the LC-tank are compensated to initiate oscillation. The former uses positive feedback to generate negative resistance whereas the latter uses capacitive division for impedance transformation and ensuring oscillation. This will be explained further in Section 4.2.2. Basic differential versions of negative-Gm and Colpitts VCOs are shown in Fig. 4.48c. For sake of completeness, it is pertinent to mention that resonators in the LC-VCOs can also be formed by quarter-wavelength ($\lambda/4$) transmission lines. Although, at mm-wave frequencies the length of such Tlines can be small enough for integration; however, careful characterization and modeling is required before their utilization in actual circuits. Therefore, VCOs based on transmission lines are not treated in this book as the number of dry runs (and design time at hand) was limited.

In recent years, the availability of advanced CMOS technologies coupled with innovative circuit and layout techniques have assisted in demonstrating LC-VCOs

operating in excess of 100 GHz [45, 93–97]. Therefore, the VCOs designed and implemented in this work are different flavours of LC based VCOs. The next section will review some basic properties of LC-VCOs with special focus on the challenges for mm-wave implementation.

4.2.2 Theoretical Analysis of LC-VCOs

Oscillators in general can be analyzed by modeling them either as feedback systems or as negative resistance model. In the latter model (details of these two approaches are presented in Appendix 2) the oscillator can be divided into two parts, a resonator and an active circuit block. An ideal resonator can sustain its oscillation indefinitely. However, in practice some of the energy circulating in the tank is lost in its resistance R_p in every cycle, thus ceasing the oscillation with time. If an active circuit connected to the resonator, generates a resistance equal to $-R_p$, the loss of the tank can be compensated and a sustained oscillation can be achieved. In other words, the energy lost in R_p is replenished by the active circuit in every cycle.

It is evident that in order to ease oscillation start-up, the loss in the resonator should be as small as possible. This loss is quantified by the well-known quality factor (Q-factor) of the tank and is given by (also derived in Appendix 2)

$$Q_{\text{tank}} = \frac{Q_C Q_L}{Q_C + Q_L} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{4.33}$$

where Q_c and Q_L are the Q-factors of the capacitive part and inductor, respectively. Equation (4.33) provides a few insights about the dependence of tank Q-factor on individual Q-factor of its components. Firstly, the overall Q-factor is the parallel combination of individual Q's of the capacitor and inductor, and secondly, the smaller of the two will dominate the overall tank Q-factor. As an example, it can be observed that at lower frequencies (up to a few gigahertz) the inductor Q-factor is lower than the capacitor (varactor in most cases) Q_C, thus dominating the circuit performance. On the other hand, at higher frequencies especially in the mm-wave regime, the Q-factor of the capacitive part of the tank is much lower than the inductor and becomes the dominating factor in the overall tank Q [98]. Thus, for mm-wave VCO designs, more effort is required to improve Q_C as compared to Q_L.

The next important consideration for LC-VCOs is the tuning mechanism by which the oscillation frequency is varied. The oscillation frequency of an LC oscillator is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4.34}$$

which shows that tuning can be accomplished either by varying the inductor or the capacitor. In practice, the inductor cannot be tuned continuously in integrated circuits.

Therefore, the capacitance is commonly varied by means of varactors. The tuning range of a VCO (as locking range of frequency dividers in (4.3) can be given by

$$TR\,(\%) = \frac{\Delta f}{f_{\text{center}}} \times 100 \tag{4.35}$$

where $\Delta f = f_{max} - f_{min}$ is the maximum frequency change around the center frequency $f_{center} = (f_{max} + f_{min})/2$. Thus, TR can also be written as

$$TR\,(\%) = \frac{f_{\max} - f_{\min}}{f_{\max} + f_{\min}} \times 200 \tag{4.36}$$

It is obvious to note, that once the inductor value is fixed in an LC-VCO, the maximum and minimum frequencies correspond to the lowest and highest capacitance value of the varactor. However, in addition to the varactor a number of unavoidable capacitances of the circuit are included in the capacitive part of the tank. Termed as the fixed capacitance (C_{fix}), it contains contributions from the capacitance of the transistors (C_{tran}), interconnect parasitic capacitance (C_{par}) and the buffer capacitance (C_{buff}) which acts as a load for the VCO. These contributions are illustrated in Fig. 4.49. In order to determine the TR in terms of capacitance values, the maximum and minimum total capacitance (C_{max} and C_{min}) can be written as

$$\begin{aligned} C_{\max} &= C_{\text{fix}} + C_{\text{var}-\max} \\ C_{\min} &= C_{\text{fix}} + C_{\text{var}-\min} \end{aligned} \tag{4.37}$$

Using (4.37) and $f = \left(2\pi\sqrt{LC}\right)^{-1}$, the tuning range of (4.36) can be expressed as

$$TR(\%) = \frac{\sqrt{\frac{C_{\max}}{C_{\min}}} - 1}{\sqrt{\frac{C_{\max}}{C_{\min}}} + 1} \times 200 \tag{4.38}$$

which can be further expanded using C_{fix} and C_{var} as

$$TR(\%) = \frac{\sqrt{\frac{C_{\text{var}-\max}}{C_{\text{var}-\min}} + \frac{C_{\text{fix}}}{C_{\text{var}-\min}}} - \sqrt{1 + \frac{C_{\text{fix}}}{C_{\text{var}-\min}}}}{\sqrt{\frac{C_{\text{var}-\max}}{C_{\text{var}-\min}} + \frac{C_{\text{fix}}}{C_{\text{var}-\min}}} + \sqrt{1 + \frac{C_{\text{fix}}}{C_{\text{var}-\min}}}} \times 200 \tag{4.39}$$

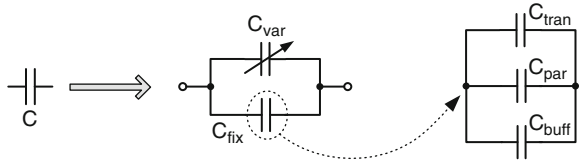

Fig. 4.49 Different contributions in the capacitive part of the LC-tank

The fixed part of the tank capacitance can be termed as the "bad-guy" in failing to achieve large tuning range, as it eats-up part of the capacitance which could have been used by varactors. Equation (4.39) clearly shows that to increase TR, the varactor capacitance ratio $C_{var-max}/C_{var-min}$ should be maximized and $C_{fix}/C_{var-min}$ should be minimized and is graphically depicted in Fig. 4.50. This is the often encountered dilemma during mm-wave VCO design. In order to ensure oscillation, large negative resistance is required, pointing to large transistor widths. However, these core transistors cannot be too large, as the fixed capacitance added to the tank reduces the tuning range. Therefore, to accommodate core transistors with a sufficient width, other parasitic capacitances connected to the tank must be minimized which provides some leverage for inclusion of larger varactors. The transistor size limitation can also be alleviated by increasing the Q-factor of the tank to lower its loss. Summarizing, mm-wave VCOs require low parasitic and high-Q resonators, as well as low parasitic and high gain transistors to satisfy the tuning range requirements.

The passive and active components constituting the VCOs introduce noise in the system. The noises of these components take various forms including shot noise, flicker noise and thermal noise. When this noise interacts with the output periodic signal of the VCO, it leads to a random variation in the output signal's amplitude and frequency. These random variations in the frequency of oscillation can also be regarded as random changes in the phase of the oscillator signal. In this case, the noise is referred to as phase noise which will be the last performance parameter of

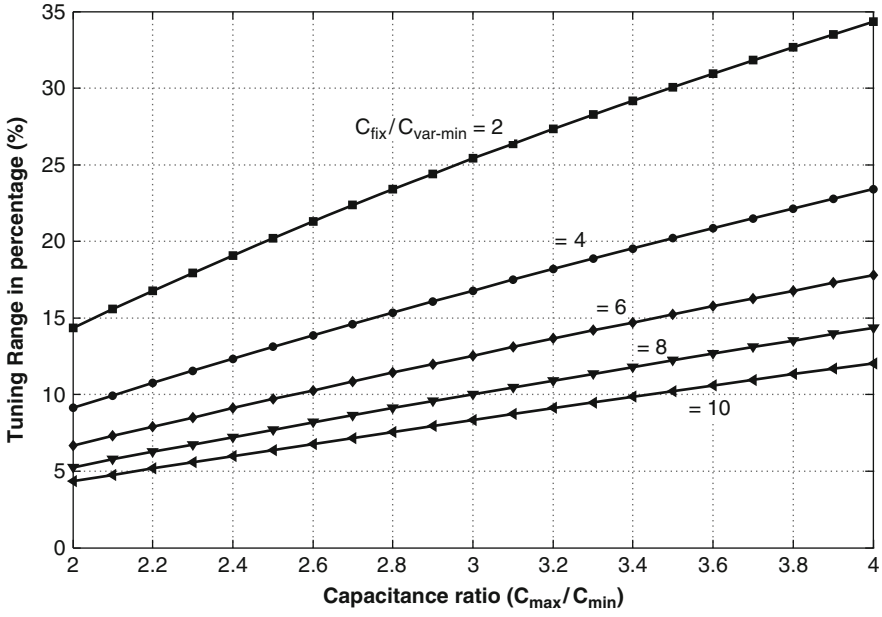

Fig. 4.50 Frequency tuning range versus C_{max}/C_{min} ratio for various $C_{fix}/C_{var-min}$

a VCO which will be considered in this section. It is one of the most important metric as it has significant influence on the overall transceiver performance. In case of frequency synthesizers, VCO phase noise determines the out-of-band noise performance as mentioned in Chapter 2, so its improvement directly affects the synthesizer noise performance.

Phase noise in oscillators has been treated extensively over the years, both theoretically as well as experimentally [99–103]. It is possible to analyze phase noise either in the frequency domain or in the time domain and both analyses are equivalent due to the duality between the two domains.

The first and quite insightful phase noise model was presented in [99] by Leeson, who quantitatively expressed the phase noise as

$$L(\Delta f) = 10 \log \left[\frac{2kTF}{P_{sig}} \cdot \left(1 + \left(\frac{1}{2Q} \frac{f_0}{\Delta f} \right)^2 \right) \cdot \left(1 + \frac{\Delta f_{1/f^3}}{|\Delta f|} \right) \right] \tag{4.40}$$

where k is the Boltzmann constant, T is the absolute temperature, $\Delta f_{1/f3}$ is the corner frequency between $1/f^3$ and $1/f^2$ phase noise regions, F is a fitting parameter that accounts for the noise of the circuit and P_{sig} is the power in the carrier signal. Based on (4.40), an asymptotic view of single-sideband phase noise is illustrated in Fig. 4.51. Three main regions exist, the close-in phase noise to the carrier is called the $1/f^3$ region and roles off with −30 dBc/decade. The $1/f^3$ region is known to be related to the up-converted 1/f noise to phase noise. The second part, which is normally dominating the phase noise spectra is called the $1/f^2$ region. Finally, at large frequency offsets from the carrier the phase noise is flat due to thermal noise. The above model shows that the dominating phase noise in the $1/f^2$ region can be improved by increasing the tank Q-factor or the carrier signal power $P_{sig.}$

Leeson's model of oscillator phase noise was based on viewing an oscillator as a time-invariant system. The main bottleneck of this model is the lack of knowledge

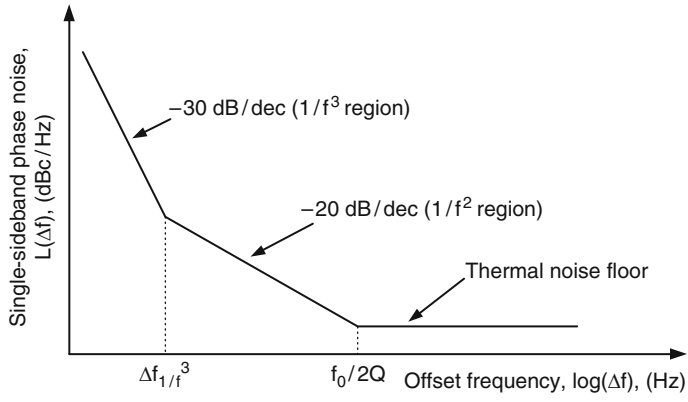

Fig. 4.51 Leeson's phase noise model

about the constant of proportionality F, which is left as an unspecified noise factor that strongly depends on the oscillator topology. Furthermore, since an oscillator is a periodically time-varying system, its time-varying nature must be included in the phase noise analysis.

There have been a number of note-worthy efforts to address the above two shortcomings. In [100], an expression for the noise factor F was derived for the negative-Gm oscillator topology of Fig. 4.48c. It was found that the bottom current source transistor is a major contributor to VCO noise and this was practically proved by a circuit implementation in [104]. Despite the additional insight gained in [100], the description of phase noise did not completely describe the physical phenomena of noise to phase noise conversion, since the time-variant nature of the oscillator was not considered. This issue was addressed in detail in [101] and proves the importance of incorporating the time-varying nature of oscillators phase noise. The key idea in this linear time-variant approach is the introduction of a function called impulse sensitivity function (ISF with symbol Γ) which quantitatively represents the varying impact of noise sources on phase noise across the oscillation period. This model provides sufficient guidelines for circuit design and predicts all regions of experimentally observed phase noise. A practical implementation of this model was presented in [105] where a low-noise Colpitts VCO (Fig. 4.48c) was optimized based on the impulse sensitivity function.

This section has provided a theoretical overview of LC based VCOs by discussing two models (feedback and negative resistance) providing the necessary conditions of oscillation. Furthermore, quality factors of the tank and underlying components are explained and higher importance of capacitor Q-factor is proven. A generalized tuning range expression is presented for LC-VCOs incorporating the fixed as well as variable (varactor) capacitances and the importance of minimizing fixed capacitance to achieve larger tuning range is highlighted. Lastly, the importance of VCO phase noise in a synthesizer and a number of prevalent phase noise models are discussed. The subsequent sections deal with the actual VCO designs for the proposed synthesizer.

4.2.3 40 GHz LC VCO

This section will present the first VCO design that will be utilized in the 40 GHz front-end of the proposed synthesizer. Recalling from Section 2.6, the two main specifications for this VCO are the tuning range of 38–42.3 GHz and a phase noise better than −100 dBc/Hz at 1 MHz offset.

Among the LC-VCO topologies, the negative-Gm topology is chosen for this design due to its simple structure and easily available differential outputs. The losses of the resonator in this topology are compensated by placing transistors in positive feedback (cross-coupled) which generates the required negative resistance to initiate oscillation. The availability of NMOS and PMOS devices implies that three different set-ups are possible: only-NMOS cross-coupled, only-PMOS cross-coupled and a

combination of the two, called the complementary cross-coupled architecture. As compared to an NMOS-only VCO, the complementary structure provides higher transconductance at a given current, which results in faster switching of the cross-coupled pair. In addition, it demonstrates superior rise- and fall-time symmetry resulting in less up-conversion of 1/f noise [80]. The combination of NMOS and PMOS transistors generates almost double the negative resistance as compared to an NMOS-only (or PMOS-only) structure, thus reducing the power consumption by half, for the same negative resistance. The evident penalty of the complementary structure is the introduction of extra device capacitances (due to PMOS transistors) as compared to an only-NMOS counterpart. In this design, the complementary structure is chosen to take advantage of the extra negative resistance for a reasonable current consumption.

The schematic of the VCO, in Fig. 4.52, shows transistors M1–M4 forming the active part, the tank inductor L_{Tank} and the tuning block which will be discussed shortly. The fixed capacitance of the VCO constituted by the transistors, buffer and layout parasitics is also shown in grey. Designing for a 0-dBm buffered output signal in a 50 Ω load, an important step is to determine the maximum and minimum capacitance required in the tank. To this end, transient and PSS simulations in Cadence™ are carried out to determine the output amplitude and oscillation frequency of the circuit. A single-turn top-metal inductor (of 95 pH) close to the minimum dimensions allowed in the technology is fixed as the tank inductor. Next, a single capacitor is used in the tank, and its value is varied to achieve the required boundary values of the oscillation frequency. For a frequency of 38–42.3 GHz, the needed capacitance is from 65 to 30 fF. On the contrary, calculations based on (4.34) show that a capacitance of 184–149 fF is required for the same frequency range. This point to the considerable amount of fixed capacitance of 119 fF present in the circuit. The break-up of this value into individual contributions is also estimated by simulations and amounts to 95 fF for the VCO transistors M1–M4, 14 fF for the buffer transistors, and the remaining 10 fF is added as an estimate of

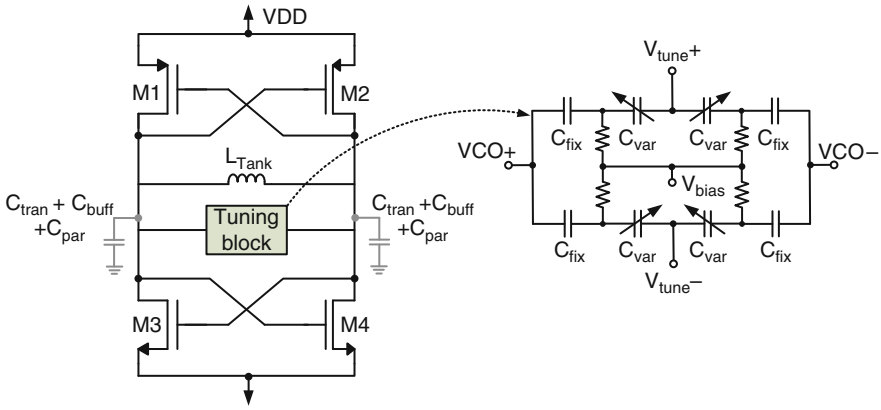

Fig. 4.52 Forty gigahertz LC VCO with tuning circuit

the layout interconnect parasitic capacitance. This analysis shows that a C_{max}/C_{min} ratio of 2.16 is required from the varactor tuning circuit to achieve the desired tuning range.

In recent years, MOS based varactors have become the default choice in comparison with diode based varactors for high frequency VCOs, due to their higher capacitance ratio and comparable (or better) Q-factor. Such a MOS varactor is formed by connecting the transistor drain and source together forming one terminal and the gate as the second terminal. The inherent transistor capacitance is then varied by applying a voltage at the gate terminal. The available CMOS technology in this work offers a modified version called accumulation MOS varactors, often referred to as AMOS varactors. In this type, the first terminal is formed by the bulk connection and the second is the gate connection as before. This marginal variation in the structure (and change in biasing) results in a larger capacitance ratio and lower parasitic resistance (thus higher Q-factor) as compared to the standard version. This has been treated sufficiently in [106–109].

To achieve the required capacitance ratio with sufficient Q-factor, the setup in Fig. 4.53a is simulated. Two AMOS varactors are connected back-to-back so that the capacitance variation is symmetric at both ends of the varactors which are connected to the VCO outputs. This setup provides the C_{max}/C_{min} ratio of 3.2 which easily satisfies the requirement. However, the Q-factor for low tuning voltages is around 4. This inhibits the oscillation for V_{tune} between 0 and 0.4 V. A simple solution is to increase the transistor size to provide more negative resistance but this increases C_{fix} and decreases the required C_{var} which is already quite small. Therefore, an alternative setup of Fig. 4.53b is considered in which a fixed MIM capacitor is added in series with the varactor on either side. As MIM capacitors have high Q-factor, they improve the overall Q-factor of the setup to a minimum of 9 and maximum of 17. The penalty paid is the reduced C_{max}/C_{min} ratio of 2.01.

The phase noise of a VCO is affected by a number of noise mechanisms, one of which is the up-conversion of low-frequency noise close to the carrier frequency. The non-linearity of the circuit can be one reason of this up-conversion, whereas the low-frequency noise can also modulate the varactors directly and appear as phase

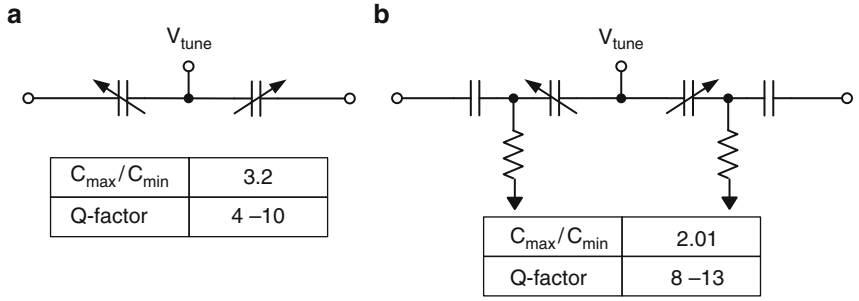

Fig. 4.53 Single-ended tuning setups with C_{max}/C_{min} and Q-factor: varactors only (**a**), and varactors with fixed capacitors (**b**)

noise close to the carrier. It can be noted that the tank inductor acts as a short circuit at low frequencies. Therefore, the noise appearing at the two outputs of the VCO around the varactor can be considered as common-mode noise. If this noise is injected into the varactors, it is up-converted to the carrier frequency by modulating the resonator. Similarly, the noise on the supply lines appear as common-mode to the varactor set-up. To alleviate this issue, a neat solution is to adopt differential tuning for the varactor setup which rejects the common-mode noise and improves the phase noise performance of the VCO.

A differential varactor setup is shown in Fig. 4.54a in which two oppositely oriented back-to-back varactors are connected across each other. The varactors labeled C_{var+} have a capacitance that decreases with the tuning voltage while the varactors labeled C_{var-} increase with tuning voltage. If a differential voltage is applied, C_{var+} and C_{var-} see positive and negative voltage respectively. Thus, both varactors are decreased in capacitance for an increase in differential input voltage. On the other hand, for a common-mode voltage the increase in C_{var+} is matched by an equal decrease in C_{var-} (or vice-versa), thus cancelling out the effect. This implies that low frequency noise voltages (1/f noise from the transistors or bias circuit, supply noise) is rejected by this varactor configuration, thus effectively improves phase noise. A number of published works [110–113] have experimentally proven the improvement of phase noise using differential over single-ended tuning. In [111], a 9 dB improvement for a 4.75 GHz VCO is reported, whereas [110] reports a 14 dB improvement for a 44 GHz VCO. Therefore, differential tuning to improve phase noise and fixed MIM capacitors to improve Q-factor is adopted in this work to arrive at the final tuning circuit of Fig. 4.54b. Resistors are used to bias the floating-nodes between the varactors and fixed capacitors. It is observed that instead of grounding the second terminal of these resistors, an external voltage (V_{bias}) provides another degree of freedom to achieve some

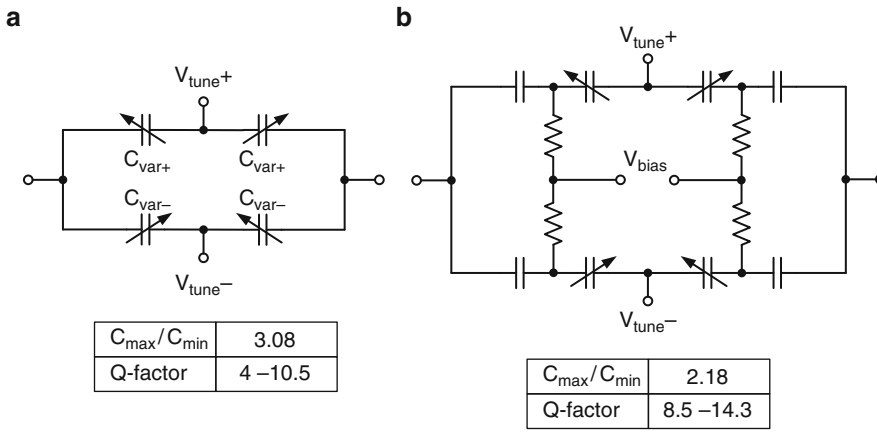

Fig. 4.54 Differential tuning setups with C_{max}/C_{min} and Q-factor: varactors only (**a**), and varactors with fixed capacitors (**b**)

capacitance tuning. Optimization based on varying the length and width of varactors as well as the fixed capacitance was carried out. The resulting varactor is composed of 15 multi-fingers, each having a length and width of 300 nm and 2 μm, respectively. The fixed MIM capacitors are 78 fF each. The C-V and Q-V curves for three different bias voltages are shown in Fig. 4.55. The tuning circuit yields a C_{max}/C_{min} ratio of 2.18 and a Q-factor between 8.5 and 14, for a differential tuning voltage of 0–1.2 V.

A number of considerations for the active part of the VCO are also important. Firstly, to ensure reliable start-up, a ratio of two is chosen between negative transconductance and losses of the tank. Secondly, to achieve gm-matching, the transconductance of the PMOS transistors is kept twice those of the NMOS transistors. A common-source differential stage is designed as an output buffer, to make on-wafer measurements possible. The buffer is biased separately to isolate its supply noise from the VCO. This also helps in measuring the power consumption of VCO and buffer separately. The load resistance (silicided polysilicon based) is 50 Ω, to match it with the transmission lines as well as the measurement equipment.

The layout of a VCO is very important for its correct performance. The basic aim is to minimize interconnect capacitance and losses. The former can shift the oscillation frequency whereas the latter can increase the risk of oscillation failure. Therefore, the core circuit including transistors, varactors and MIM capacitors is placed very close to the inductor terminals to minimize interconnect length. The core layout is RC extracted and shows a shift in oscillation frequency. Therefore,

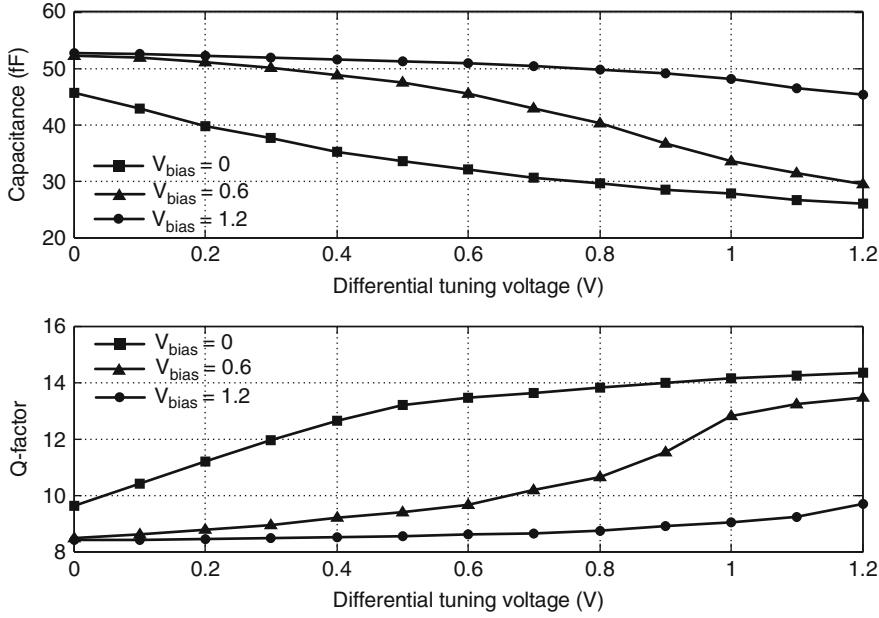

Fig. 4.55 Capacitance (*top*) and Q-factor (*bottom*) of the tuning circuit for 40 GHz VCO

the capacitance of the tuning part is adjusted accordingly and is about 13 fF lower than the required capacitance on the schematic level. Ground meshing is used underneath and between RF paths and decoupling capacitors are included for the voltage supplies of the VCO and buffer. The differential outputs from the output buffers use 50 Ω transmission lines (TLs) to the bond-pads. These TLs are coplanar waveguide based with lateral ground-plane consisting of all metal layers. The width of the signal line is 5 μm and the spacing from the 10 μm wide ground plane is 4.22 μm. The VCO is fabricated in the same technology as the ILFDs presented in Section 4.1. The bond-pad limited chip area is 700 × 400 μm^2 whereas the VCO core only occupies 100 × 100 μm^2. The chip micrograph is shown in Fig. 4.56.

The VCO was measured on-wafer using a high frequency differential probe (GSGSG) and a 180° hybrid (ET industries). An Agilent PSA series spectrum analyzer with phase noise functionality was used for spectral measurements. The measurement equipment generates considerable external noise, which could potentially degrade the measured results. In order to suppress the noise coming from power supplies, dedicated filters are employed. In addition, common-grounds between the supplies and spectrum analyzer are eliminated. The lighting of the viewing optics is turned-off during measurement [110]. It is noticed that central alignment of the infinity probes (on the bond-pads) and good probe contact yield stable and repeatable measurements.

The VCO starts to oscillate for a supply voltage as low as 1 V but the desired output power is obtained at 1.2 V. The VCO is biased at 3 mA, whereas the output buffer consumes 5 mA. The resulting power consumption is 3.6 and 6 mW respectively. The differential tuning voltage is then applied to the tuning circuit to measure the frequency tuning range (FTR). The lowest measured frequency of 41 GHz is obtained for a differential voltage of 0 V and V_{bias} equal to 1.2 V. On the other hand, the maximum frequency of 44.5 GHz is achieved with 1.2 V differential tuning voltage and $V_{bias} = 0$ (spectrum screen-shot close to maximum frequency is shown in Fig. 4.59a). The center frequency is thus 42.75 GHz. The frequency versus

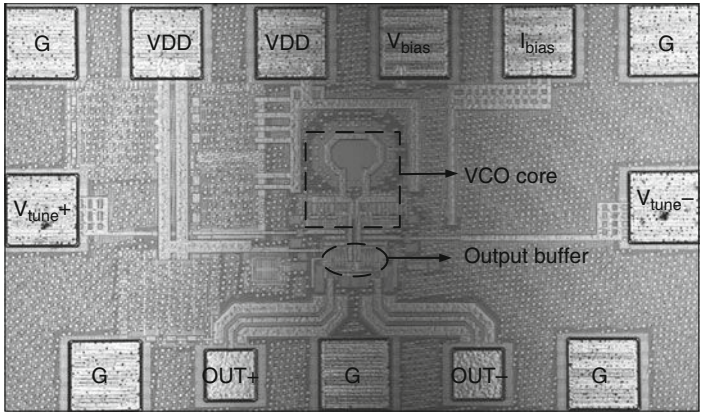

Fig. 4.56 Chip micrograph of 40 GHz LC VCO

differential tuning voltage of 0–1.2 V for three different values of V_{bias} is shown in Fig. 4.57. The average FTR for each V_{bias} is 2 GHz and a total FTR of 8.2% (3.5 GHz) is achieved. The total loss from the wiring cables, connectors and hybrid was measured between 6 and 8 dB over the entire frequency tuning range. After de-embedding this loss, the average differential output power of the VCO delivered to a 50 Ω load is between −2 and −6 dBm as shown in Fig. 4.58.

The phase noise of the VCO is measured using the same spectrum analyzer at different frequencies within the FTR. At 41.2 GHz (close to the lower end of the tuning range) the measured phase noise at 1 MHz offset is −106.3 dBc/Hz (Fig. 4.59b) which is the lowest over the FTR. At the center frequency of 42.75 GHz, the phase noise is −104.8 dBc/Hz, whereas at 44.1 GHz (upper end of the FTR) the phase noise of −102.5 dBc/Hz at 1 MHz is the highest among all the values.

There are two commonly adopted figures of merit (FOM) for VCOs. The first one called the phase noise FOM, allows comparison of oscillators running at different oscillation frequencies with their phase noise measured at certain offsets. Furthermore, it also accounts for the DC power consumption of the VCO as phase noise can be improved by burning more power in the VCO. The resulting FOM in dBc/Hz is given by

$$FOM_{PN} = L(f_0, \Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1\,mW}\right) \tag{4.41}$$

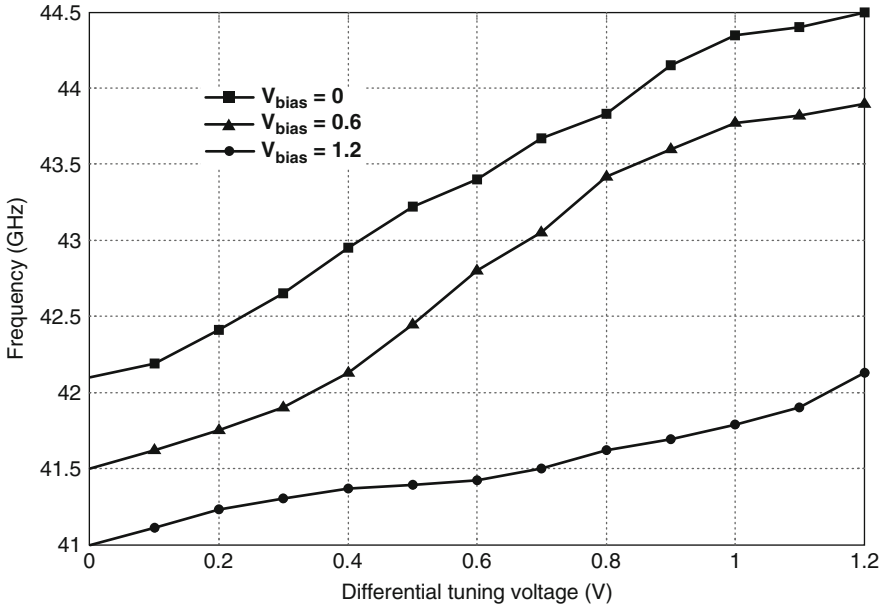

Fig. 4.57 VCO frequency tuning range

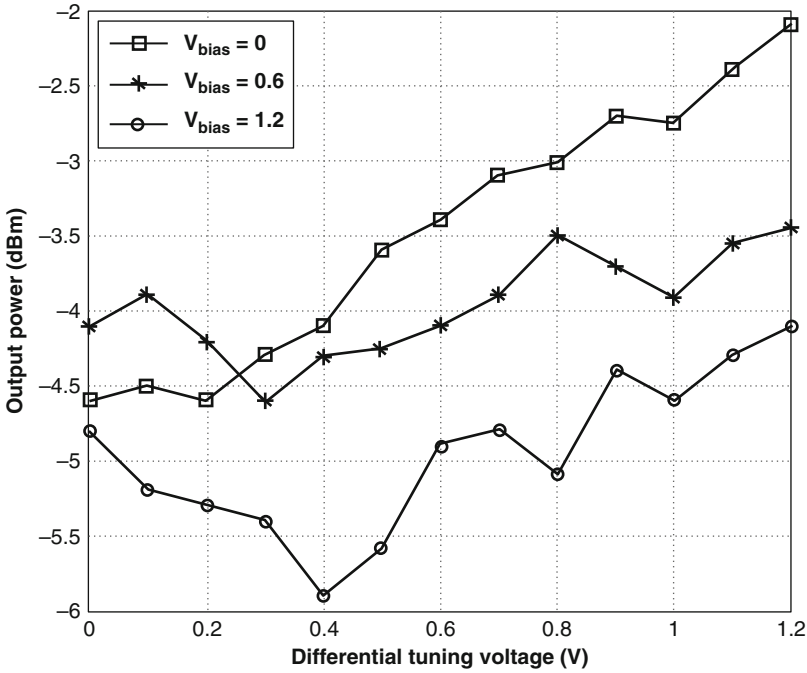

Fig. 4.58 VCO output power after de-embedding cable and measurement loss

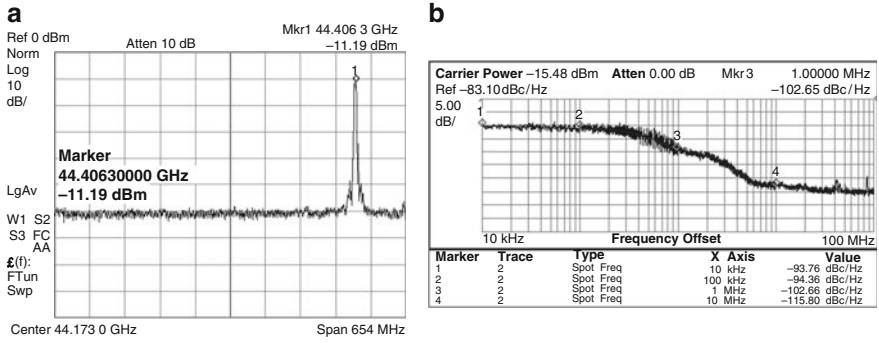

Fig. 4.59 VCO spectrum at 44.4 GHz (**a**), and phase noise for a 44 GHz oscillation frequency (**b**)

where $L(f_0,\Delta f)$ is the single-side-band phase noise at a frequency offset Δf from a carrier at f_0, and P_{DC} is the DC power consumption. A lower FOM_{PN} (i.e. a more negative value) indicates a better VCO. Using (4.41), the FOM_{PN} for the lower, middle and upper ends of the FTR is −192.7, −191.8 and −189.8 dBc/Hz, respectively.

Achieving a wide tuning range is a considerable challenge for mm-wave VCOs, thus for a fair comparison, the second FOM incorporates the achieved tuning range of the VCO and is given by

$$FOM_{FTR} = L(f_0, \Delta f) - 20\log\left(\frac{f_0}{\Delta f} \cdot \frac{FTR}{10}\right) + 10\log\left(\frac{P_{DC}}{1\,mW}\right) \tag{4.42}$$

where FTR is the tuning range in percentage and rest of the parameters are the same as in the FOM_{PN}. Again, a lower FOM_{FTR} indicates a better VCO. The FOM_{FTR} values for the VCO at the lower, middle and upper ends are −191.3, −190.1 and −188.1 dBc/Hz, respectively. The VCO is compared with some published works in Table 4.3.

The measurement results of the presented 40 GHz VCO show that the over-design adopted, based on the RC extraction, resulted in a higher oscillation frequency than desired; the RC extracted simulation results are often found to be pessimistic. The measured FTR of 8.2% also fell short with respect to the desired 10% to cover the 38–42.3 GHz frequency range. The phase noise target specification of −100dBc/Hz was met successfully over the complete tuning range. Nevertheless, the insight gained during the step-by-step design procedure of the VCO enables the correction of these parameters in subsequent integration in the frequency synthesizer.

4.2.4 60 GHz Actively Coupled I-Q VCO[2]

This section is dedicated to the voltage controlled oscillator for the 60 GHz front-end of the proposed synthesizer. The synthesizer's application in a direct-conversion receiver necessitates the need of quadrature outputs from the VCO. The specifications laid out in Chapter 2 require a tuning range of 57–63.6 GHz

Table 4.3 Comparison of 40 GHz VCO with published works

Reference and technology	Frequency (GHz)	P_{DC} (mW)	FTR (%)	PN @ 1-MHz (dBc/Hz)	FOM_{PN} (dBc/Hz)	FOM_{FTR} (dBc/Hz)
[97] 0.13 μm CMOS	59.0	9.8	10.2	−89.0	−174.5	−174.6
[98] 0.13 μm CMOS	43.0	7.0	4.2	−90.0	−174.2	−166.7
[110] 0.12 μm SOI CMOS	44.0	7.5	9.8	−101.8	−185.0	−184.8
[114] 0.13 μm SOI CMOS	40.7	11.3	15	−89.0	−171.6	−170.6
[115] 0.18 μm CMOS	50.0	4.0	2	−96.0	−184	−170
Section 4.2.3 65 nm CMOS	44.5	3.6	8.2	−106.3	−192.7	−191.3

[2]This design, published in [28], was carried out in cooperation with Pooyan Sakian, who is the first author of this publication.

(10.94%) and a phase noise better than −90 dBc/Hz at 1 MHz offset. Achieving more than 10% FTR at 60 GHz in bulk CMOS technology and providing I-Q outputs at the same time is a considerable task. Furthermore, due to the pronounced effect of parasitics at these frequencies, hitting the exact required frequency is another challenge. In order to achieve an FTR in excess of 10%, published works have predominantly relied either on specialized technologies such as SOI [116, 117] or on using two VCOs to cover the complete 60 GHz ISM band [118].

The quadrature outputs from a VCO can be obtained by using poly-phase filters or by coupling two independent VCOs actively or passively. The pros and cons of these methods were discussed in Section 4.2.3 where a 40 GHz ILFD was designed for quadrature operation. The experience gained during that design with good measured results, helped in using the actively coupled method for the 60 GHz VCO with two evident differences. Firstly, the core of the VCO needs to operate at 60 GHz instead of ∼20 GHz and secondly, no injection transistors are needed as the two VCOs will be free-running in the 60 GHz band. The first difference is an important one, as the required tank capacitance and inductance have to be considerably small, to ensure a 60 GHz oscillation frequency. Furthermore, the fixed capacitances emanating from the active devices, output buffers and interconnect parasitics become the bottle-neck to achieve the desired tuning range and have to be minimized as depicted by formula (4.39).

The VCO circuit schematic is shown in Fig. 4.60a. The active part generating the negative resistance to compensate tank losses is formed by minimum length transistors M1–M4. The tank is constituted by a center-tapped single-turn octagonal inductor and AMOS varactors. The former has an inductance of 72pH and a Q-factor of 15 at 60 GHz. The signal trace width is 4.42 μm with an inner diameter of 33 μm and is surrounded by a guard-ring. The varactors used in this design are tuned single-endedly as the differential tuning circuit in Section 4.2.3 contributes to the fixed capacitance which cannot be afforded in this design due to the high frequency. The varactors have a multi-fingered structure and are optimized for high-enough Q-factor and minimum fixed capacitance. Each varactor has 36 fingers which are 1.5 μm and 280 nm in width and length, respectively. The maximum and minimum varactor capacitance is 47.8 and 17.8 fF, resulting in a C_{max}/C_{min} ratio of 2.7. The Q-factor of the varactors at 60 GHz ranges from 5 to 15 depending on the tuning voltage.

The coupling transistors M5–M8 inject the output signals of one cross-coupled pair to the other to produce anti-phase coupling required for quadrature generation. As these transistors add extra fixed capacitance (thus reducing FTR) to the oscillation nodes, they should be small. However, making them too small results in the injection becoming weaker and the risk of frequency mismatch between the two tanks is increased. Therefore, the dimensions of the coupling transistors are optimized to provide sufficient injection for accurate quadrature outputs while adding minimum parasitic capacitance to the tank. The resulting W/L of the coupling transistors is one-fourth of the VCO transistors. The bias current is provided by a current-mirror circuit (not shown) using transistors which have three-times the minimum length of the technology. This lowers their flicker noise which could potentially be up-converted appearing as phase noise around the carrier. The output

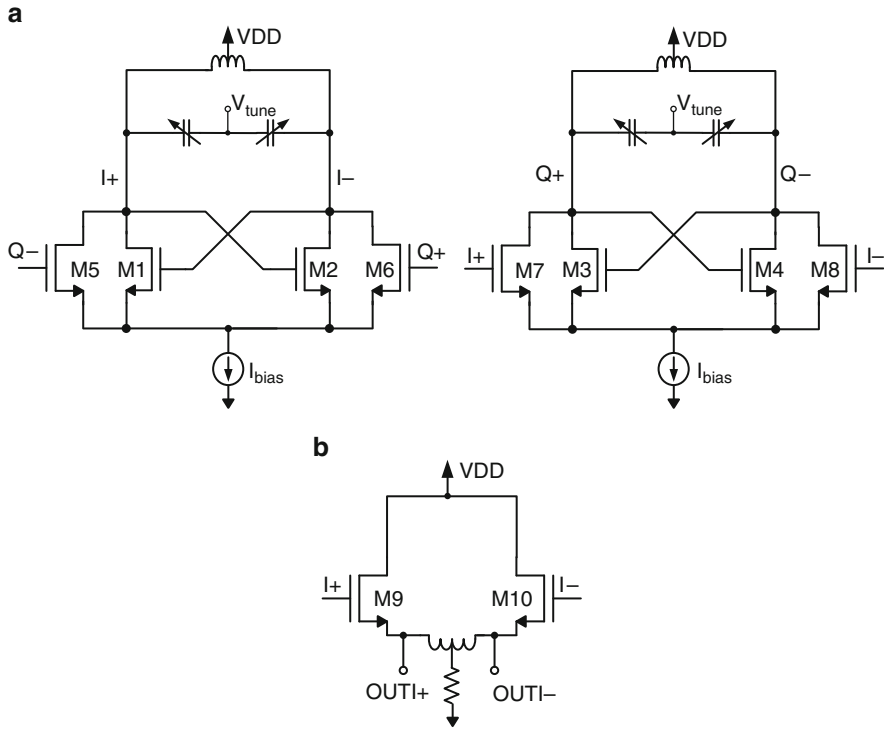

Fig. 4.60 Sixty gigahertz actively coupled I-Q VCO (**a**), and source follower output buffer (**b**)

buffer used in this design is a source-follower as shown in Fig. 4.60b. It includes a center-tapped inductive load and minimum-length transistors to avoid excessive loading of VCO outputs. The resistor in the common source node of the buffer determines the biasing current of the differential pair. The gate of M9 and M10 can be connected directly to the output of the VCO, avoiding large RF-coupling capacitors.

The importance of layout symmetry to maintain quadrature accuracy was discussed in Section 3.1.2. In this design, special attention is paid to the symmetry of the layout to minimize the phase mismatch between I and Q outputs. The core transistors including cross-coupled pairs and injection transistors are arranged in a symmetrical ring configuration. While providing very good symmetry for the connections, this arrangement suffers from a mismatch in the orientation of the transistors and varactors. On the other hand, arranging the transistors in an orientation-matched configuration, would introduce a length mismatch in the interconnects which can increase the phase mismatch. Therefore, the former approach has been selected in this work. Coupling between inductors of the two tanks is another potential source of phase mismatch. To minimize this effect, they are placed perpendicular to each other and meshed grounding is utilized around the inductors to confine the magnetic fields within a small area. The phase error between the

quadrature outputs in post-layout (RC extracted) simulations is less than 1° over the complete tuning range. The differential I-Q outputs utilize 50 Ω transmission lines from the output buffer to the bond-pads. The circuit is fabricated in 65 nm bulk CMOS process and the chip micrograph is shown in Fig. 4.61. The core circuit including the VCO and output buffers occupies 300 × 300 μm^2 and the total chip area is 800 × 825 μm^2.

The measurements are performed on-wafer with high-frequency GSGSG Infinity probes. Specialized waveguide based connectors and differential to single-ended converters (Magic-T) are employed for rigidized and stable connection. As the maximum frequency of the spectrum analyzer is below 50 GHz, an Agilent V-band (50–75 GHz) harmonic mixer 11970V is used in combination with the spectrum analyzer for viewing the 60 GHz signal. The setup for the spectrum measurement is shown in Fig. 4.62a. The noise floor of the spectrum analyzer is increased considerably due to the harmonic mixer; hence, the phase noise measurement using the option provided by the SA does not yield reliable results. Therefore, an indirect method is adopted to measure the phase noise. The 60 GHz RF signal is down-converted using an external mixer (Marki Microwave M9-0465) with the LO signal provided by a signal generator (E8361 PNA). The down-converted signal below 7 GHz is applied to an Agilent signal source analyzer (E5052) which offers an ultra low noise floor and provides accurate phase noise measurements. The phase noise measurement setup is depicted by Fig. 4.62b.

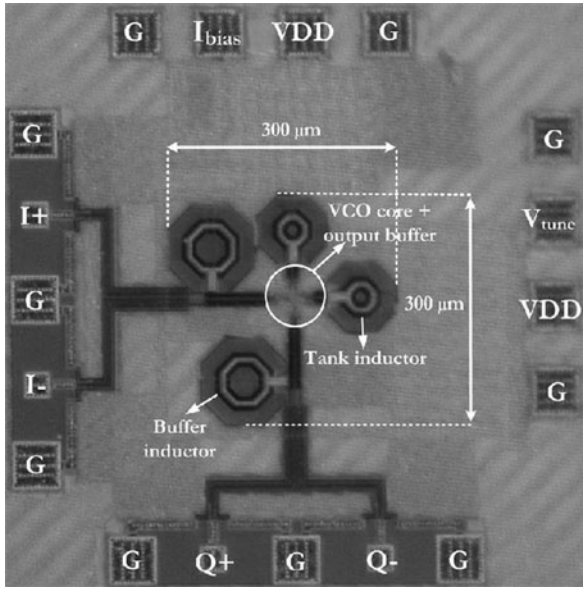

Fig. 4.61 Chip micrograph of the 60 GHz actively coupled I-Q VCO

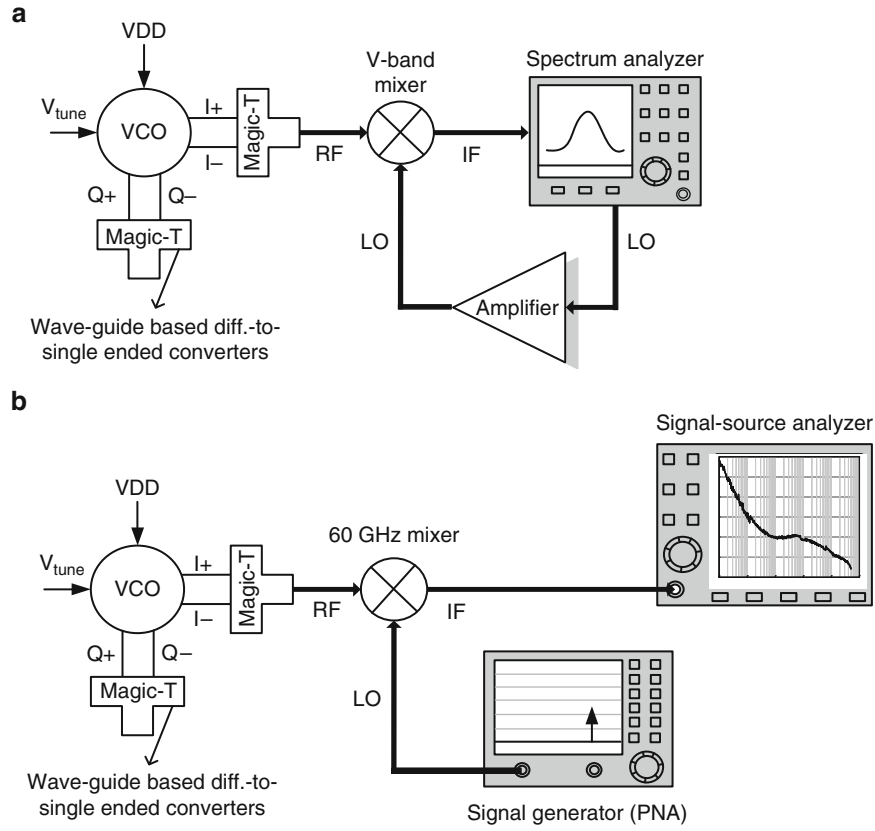

Fig. 4.62 Sixty gigahertz VCO measurement setups for spectrum measurements (**a**), and phase noise measurements (**b**)

The frequency tuning range is measured for different bias currents and shown in Fig. 4.63. During the measurements, it was noticed that the maximum variation of frequency is achieved for a varactor tuning voltage between 0.6 and 1.8 V as opposed to expected range of 0–1.2. This problem was traced back to the simulation of the varactor setup which was not biased correctly. Nevertheless, the overall voltage range is kept equal to the supply voltage (1.2 V). For the minimum current of 10mA, the lowest oscillation frequency is 57.6 GHz and the highest frequency is 63.5 GHz. On the other hand, the maximum bias current of 15 mA yields an oscillation frequency of 57.5–63.1 GHz. The average tuning range is 57.6–63.3 GHz with a center frequency of 60.4 GHz, resulting in a 9.3% tuning range. The I-Q VCO can also operate at a reduced supply voltage of 1 and 1.1V. The corresponding FTR for I_{bias} of 14 mA are 9.96% and 9.25%, respectively. Increasing the tuning voltage range from 1.2 to 1.5 V, enhances the FTR to 11.5%, with the maximum and minimum oscillation frequencies of 57.5 and 64.5 GHz. Each VCO core, including a cross-coupled pair and an LC-tank, draws 15 mA from the 1.2 V supply

(resulting in a total power consumption of 36 mW for the I-Q VCO). The two inductively-loaded source-follower output buffers consume 20 mA in total.

The phase noise is measured for a bias current of 15 mA over the complete tuning range. Shown in Fig. 4.64, the phase noise at the lower-end of the FTR (57.5 GHz) is −81 dBc/Hz and −95.3 dBc/Hz at 10 kHz and 1 MHz offset, respectively. Towards the higher end at 62.7 GHz, the corresponding phase noise values are −84.4 dBc/Hz

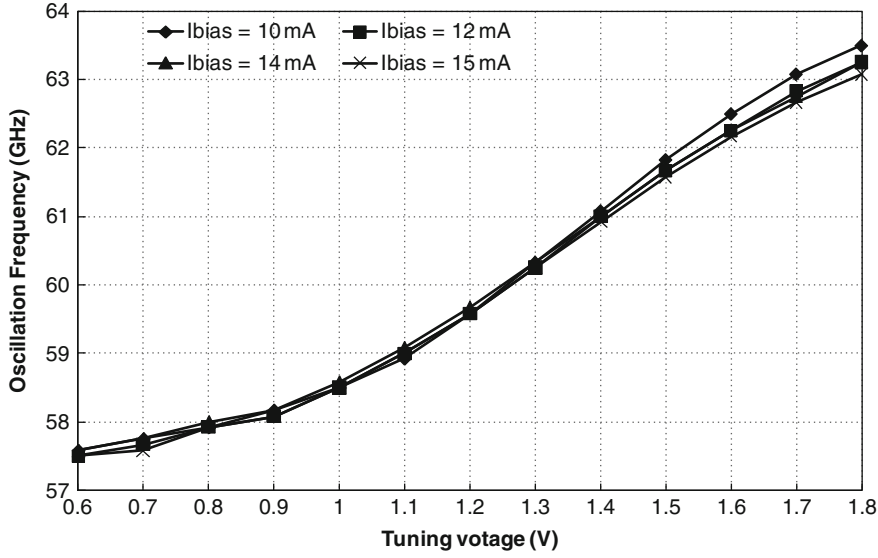

Fig. 4.63 Frequency tuning range of the 60 GHz actively coupled I-Q VCO

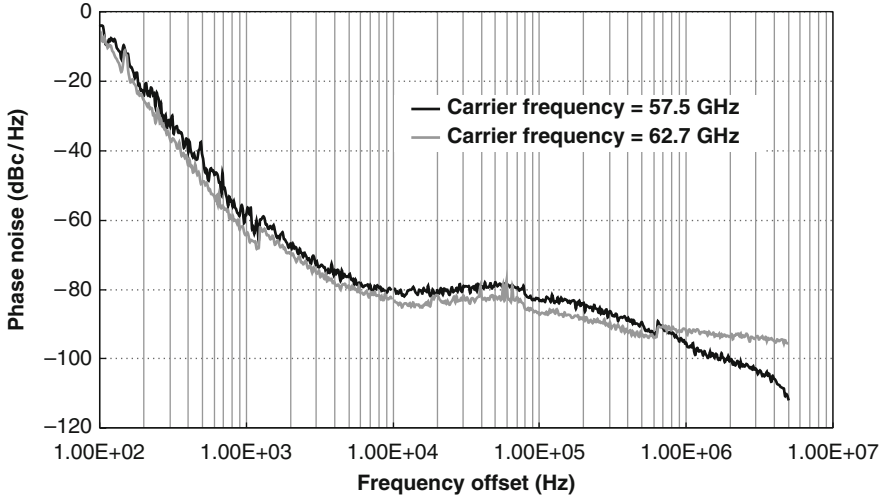

Fig. 4.64 Phase noise of 60 GHz actively coupled I-Q VCO at the lower and higher end of FTR

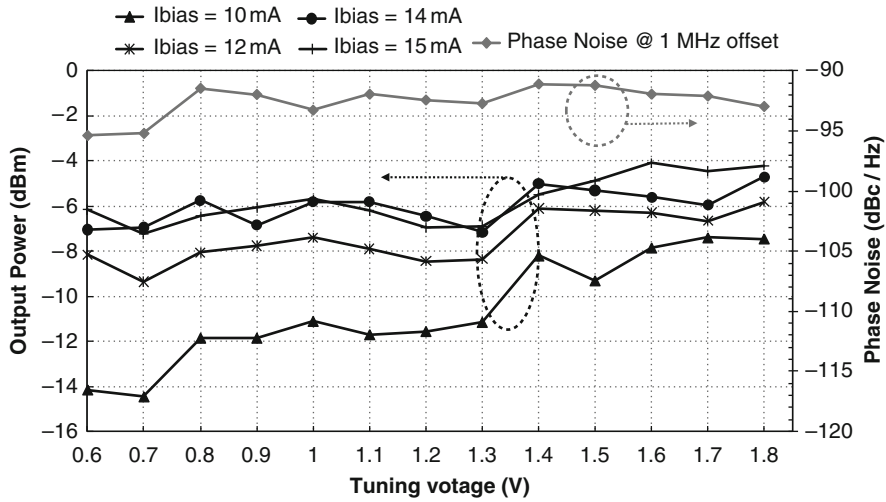

Fig. 4.65 Output power and phase noise variation of the 60 GHz actively coupled I-Q VCO over the FTR

and −92.1 dBc/Hz at 10 kHz and 1 MHz offsets. The phase noise variation over the FTR is about 4 dB, with the lowest and highest values of −95.3 dBc/Hz and −91 dBc/Hz, respectively. This is graphically shown in Fig. 4.65. The average measured phase noise is within ±2 dB in comparison with the simulated results based on completely RC-extracted circuit components. The output power variation of the I-Q VCO after de-embedding the losses of cables, connectors and other measurement equipment is also presented in Fig. 4.65. For a bias current between 12 and 15 mA, the output power lies between −4 and −9 dBm whereas for the lowest current of 10 mA the power varies between −8 and −14 dBm. The FOM_{PN} and FOM_{FTR} based on the measured values are −174.9 and −174.3 dBc/Hz, respectively.

The 60 GHz I-Q VCO satisfies the target specifications quite closely and exhibits comparable performance to state-of-the-art single-phase VCOs, despite the additional challenges and limitations imposed by the quadrature topology. The average FTR is 9.3% and with a tuning voltage extended to 1.5V, the achieved FTR is 11.5% in comparison to the required 10.9%. The phase noise over the complete FTR is better than the required −90 dBc/Hz at 1 MHz offset. The output power of the VCO is sufficient to drive the 60 GHz ILFD of Section 4.1.4 or the dual-mode ILFD of Section 4.1.6.

4.2.5 60 GHz Transformer Coupled I-Q VCO

This section presents another approach to achieve quadrature operation for a 60 GHz VCO. Active coupling using transistors in parallel (or series) with the cross-coupled pair, although offers a simple and robust method to generate 90° spaced outputs, has

a few drawbacks as well at mm-wave frequencies. Firstly, as mentioned in the preceding section, the coupling transistors contribute to the fixed part of the tank capacitance thus wasting useful portion of the variable capacitance. Consequently, the tuning range and the operation frequency is reduced and dimensioning of the coupling transistor becomes very important. Secondly, the coupling transistors are a potential source of introducing 1/f noise which can be up-converted, appearing as phase noise close to the carrier. An alternative of inserting the coupling transistors in series [78] with the cross-coupled transistors can circumvent the phase noise degradation. However, it introduces voltage headroom limitation, making it unsuitable for low-voltage operation.

Therefore, a completely different approach to achieve quadrature operation, based on transformer coupling (TC) is presented here. This method can potentially alleviate all three disadvantages of active coupling, as it neither requires extra voltage head-room, nor does it introduce large parasitic capacitance and 1/f noise in the circuit. Furthermore, it can operate with low supply voltages along with DC power savings. Despite these ideal properties, transformer-coupled I-Q VCOs have not received much attention due to two main reasons. Firstly, at low frequencies the silicon-area penalty is considerable as up to four transformers are required to achieve quadrature outputs and secondly, the modeling and EM simulations required for the transformers increase the design time. Fortunately, the first issue of silicon-area is almost irrelevant at 60 GHz as the dimensions of required transformers are very small. For instance, an octagonal 70–80 pH coil of a transformer occupies a mere $\sim 50 \times 50\ \mu m^2$ which is close to a single bond-pad dimension. Thus, the affordability of transformers makes the transformer coupled (TC) I-Q VCO, a feasible choice.

The TC I-Q VCO can be thought of as an extension of a conventional transformer feedback VCO with differential outputs as presented in [119]. Shown on the left side of Fig. 4.66, this design employs a transformer in place of an inductor. The transformer's primary coil is connected at the transistor drain terminal forming

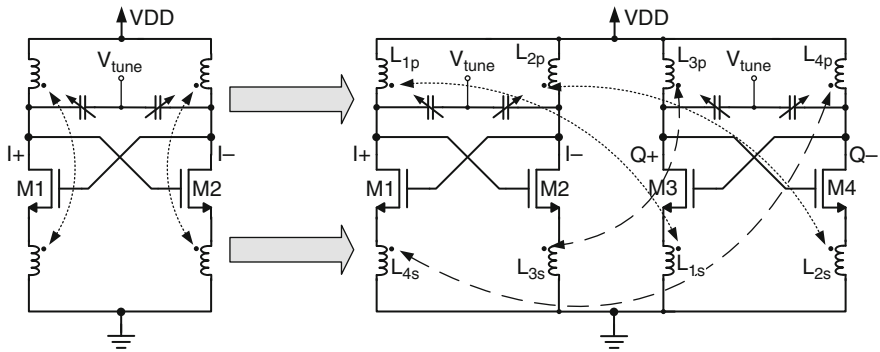

Fig. 4.66 Extension of a 60 GHz differential transformer feedback VCO to a TC I-Q VCO

an LC tank with the varactor setup. The secondary coil is connected at the source terminal and is magnetically coupled to the primary coil with a certain coupling factor. With transformer feedback, the drain voltage can swing above the supply voltage and the source voltage can swing below the ground potential. As the drain and source voltages of coupled transistors (M1 and M3, M2 and M4 and so on) are in phase, the effective oscillation amplitude is large. Consequently, VCO performance parameters can easily be traded-off according to the specifications [120]. For instance, similar phase noise performance (as a conventional VCO) can now be achieved with lower supply voltage (hence lower power consumption). Alternatively, owing to larger oscillation amplitudes, phase noise can be improved for the same power consumption.

In order to generate quadrature outputs, the right side of Fig. 4.66 shows the transformer coupled I-Q VCO in which the transformer, instead of providing feedback between drain and source of the same transistor, now couples the drain and source of two different transistors, present in separate cross-coupled pairs. The primary and secondary coils of the four transformer are numbered as L_{Xp} and L_{Xs} where X = 1, 2, 3 and 4, respectively. As an example of coupling, the primary coil (L_{1p}) of transformer L_1 in drain the of M1 couples to its secondary coil (L_{1s}) at the source of M3, which is present in the separate cross-coupled VCO. The rest of the couplings are shown by dotted and dashed lines. From the outset, it is evident that the parasitic capacitance and the noise contributed by the coupling transistors (of actively coupled I-Q VCOs) is removed, which assists in achieving higher operation frequency, larger tuning range, and lower power consumption. As with actively coupled quadrature VCOs, the circuit can be re-drawn in a ring structure to understand the quadrature operation with the difference that the two VCOs are magnetically coupled through transformers instead of transistors. The ring configuration is shown in Fig. 4.67.

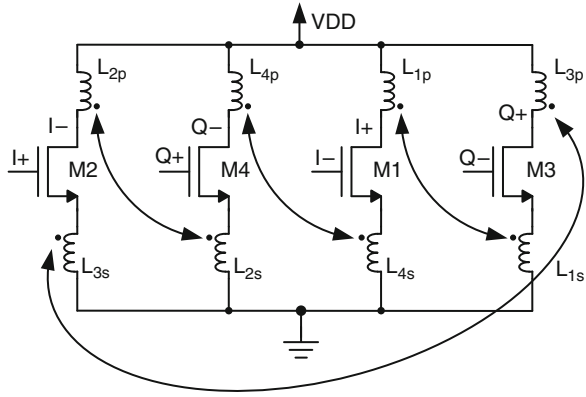

Fig. 4.67 TC I-Q VCO re-drawn in a ring structure

The circuit design of the TC I-Q VCO entails a number of steps. Firstly, simulations (in Cadence™) based on ideal transformer components (two inductors with a mutual coupling factor) are run to extract the first estimate of the required inductance and coupling factor (usually referred as 'k'). Based on these requirements, EM simulations are carried out to determine a suitable transformer structure. A lumped model fitting these EM simulations is then required to run transient simulations of the VCO. Depending on subsequent results, this process can be an iterative one until the specifications are met. As four transformers have to be used, the selection of its structure is also intertwined with the final floor-plan of the I-Q VCO. The aim should be to place the transformers in a way to ensure perfect symmetry between I and Q paths and also to minimize interconnect length at the same time.

The transformer used in the I-Q VCO was designed and measured independently, details of which were presented in Section 4.1.5. Using a lumped model fitting these values, the VCO is simulated to estimate the tuning range, phase noise and quadrature accuracy. Varactors with single-ended tuning similar to the 60 GHz actively-coupled VCO design are used. The I-Q outputs of the VCO are buffered using 50 Ω common-source differential stages for measurement purposes. As quadrature accuracy of the VCO is dependent on the layout as well, it is important to include its effect during simulations. To this end, based on the decided floor-plan of the VCO, the layout of the core active circuit and subsequent RC extraction is done. This extracted version of the circuit is utilized for final simulations.

As mentioned previously, the use of transformers provides the leverage to reduce the supply voltage, achieving a large output amplitude at the same time. This is analyzed for the I-Q VCO under discussion, by varying VDD from 0.6 to 1.2 V and observing the corresponding peak-to-peak output amplitude. Fig. 4.68 shows the said parameter for three separate values of varactor tuning voltage, V_{tune}. At a supply voltage of 0.6 V, the peak-to-peak amplitude is about 1V and increases as the VDD is incremented. At the maximum VDD of 1.2 V, the achievable amplitudes are 1.85, 2.6 and 2.94 V for tuning voltages of 0.6, 0.9 and 1.2 V, respectively. This confirms that large output signals are possible at even half the nominal supply voltage. Apparently, the minimum supply voltage of 0.6 V can be chosen as it provides sufficient amplitude but the final selection of the supply voltage also depends on the resulting phase noise of the VCO. Therefore, phase noise at 1 MHz for $V_{tune} = 1.2$ is also plotted in Fig. 4.68. It is observed to vary between −89.8 and −97.4 dBc/Hz for supply voltage between 0.6 and 1.2 V respectively. As the target phase noise for the I-Q VCO is −90 dBc/Hz, so a supply voltage of 0.8 V is chosen as a final design value. At this VDD, the phase noise is −94 dBc/Hz, which satisfies the above target with some margin (keeping in view the difference between simulations and measurements). The I-Q VCO consumes 29.2 mA, resulting in a power consumption of 23.3 mW, which is lower than the 36 mW consumed by the actively coupled VCO of Section 4.2.4.

The frequency tuning range of the TC I-Q VCO is plotted in Fig. 4.69 for different supply voltages. The minimum and maximum oscillation frequencies are placed slightly higher than the required ones, anticipating the frequency shift

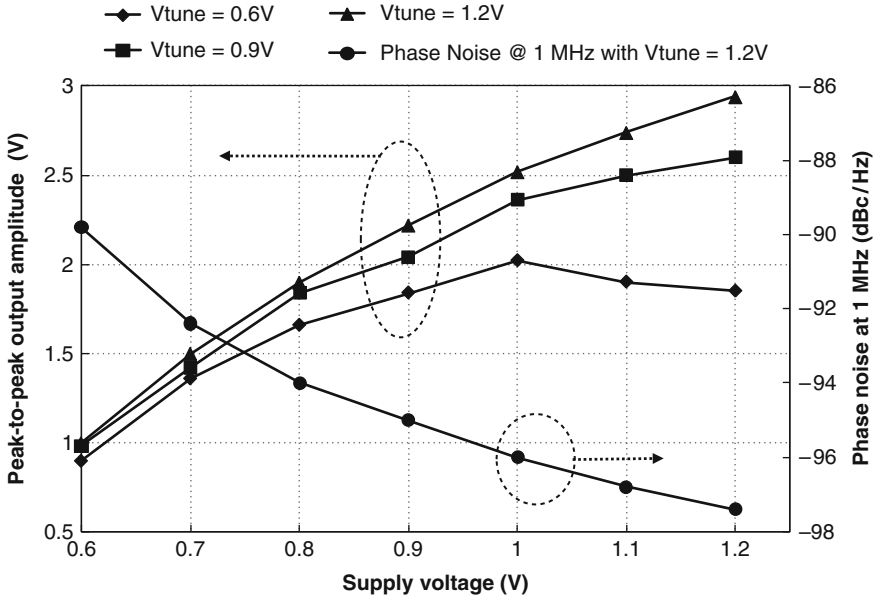

Fig. 4.68 Variation of output amplitude and phase noise of the 60 GHz TC I-Q VCO

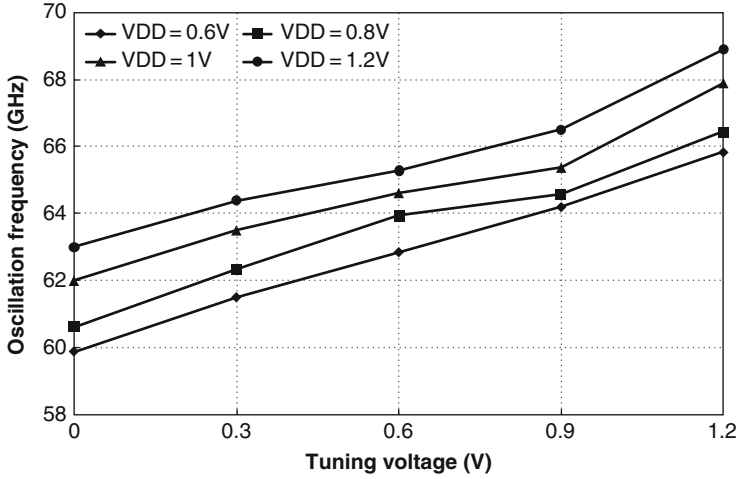

Fig. 4.69 Frequency tuning range of the 60 GHz TC I-Q VCO

visible in earlier measured results. The average FTR for all supply voltages is about 10% which is close to the target FTR of 10.9%. The quadrature accuracy or phase-error between I and Q outputs can also be estimated by output waveforms of

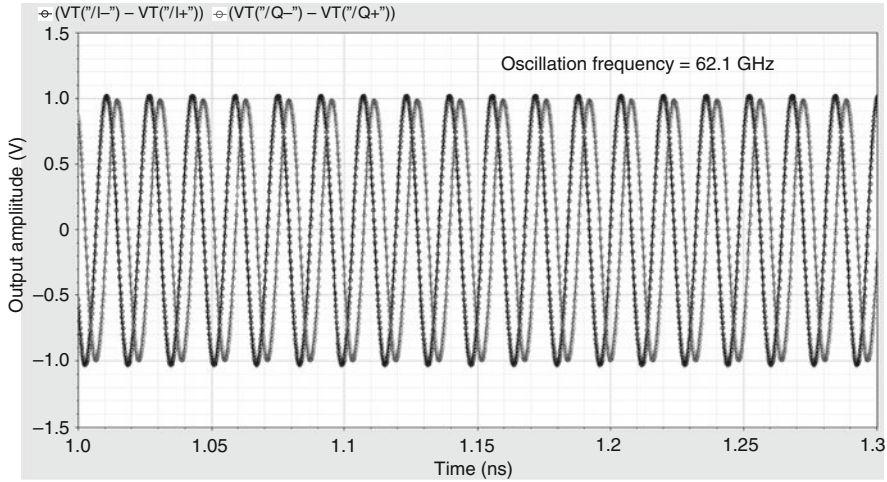

Fig. 4.70 Quadrature outputs at 63 GHz of a TC I-Q VCO

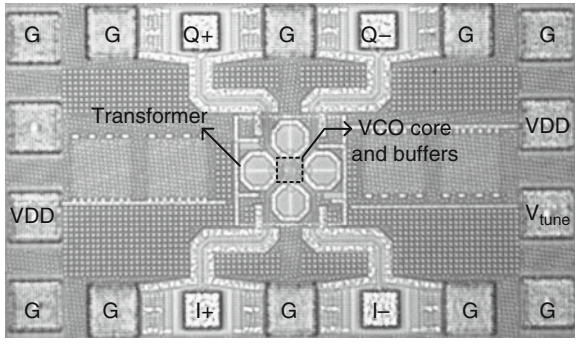

Fig. 4.71 Chip micrograph of 60 GHz TC I-Q VCO

transient simulations. One such a plot is shown in Fig. 4.70, for an oscillation frequency of 62.1 GHz. The average phase error over the complete tuning range is less than 1°. The FOM_{PN} and FOM_{FTR} based on the above post-layout results are both −176.8 dBc/Hz.

The chip micrograph of the TC I-Q VCO is shown in Fig. 4.71. The four transformers are placed in a circular fashion with the core circuit, constituting the VCO transistors and output buffers, placed in between them. The varactors are placed between the transformer terminals to minimize the interconnect between them. The outputs from the buffers are fed to 50 Ω transmission lines. The dimension of each transformer is 54 × 52 μm^2 and it is evident that the silicon area consumed by them is not considerable. The layout is symmetrical from all sides, so-much-so that during wafer-probing it was difficult to identify the correct

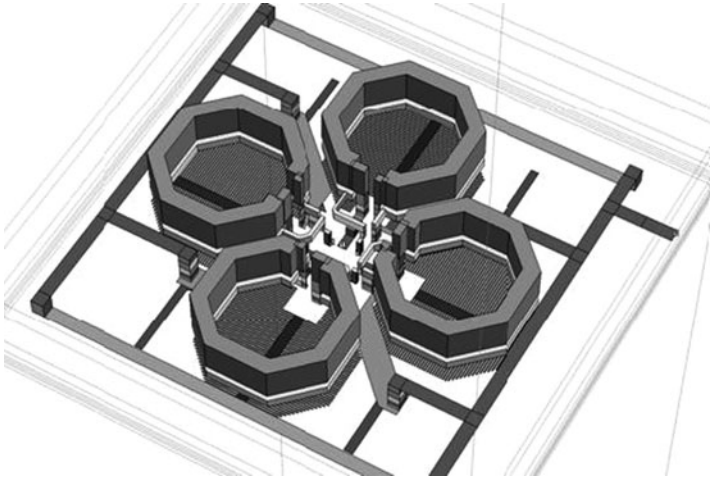

Fig. 4.72 Core circuit layout exported into Sonnet

orientation for biasing the circuit properly. The setup for spectrum measurements is identical to the one explained in Section 4.2.4 and depicted in Fig. 4.62a.

Despite the promising post-layout simulation results, the actual measurements had a different outcome. The DC conditions exactly matched the simulations showing that the circuit connections and fabrication were correct. However, no oscillation was visible on the spectrum analyzer. The supply voltage as well as the varactor tuning voltage was varied within tolerable range but it did not help to "kick-start" the oscillation. One potential reason for the non-oscillatory behavior is thought to be the interaction of the four transformers with each other due to their close proximity. The simulations included lumped models of each transformer, but the actual situation where four transformers are placed close to each other was not mapped into the simulations.

In order to investigate this reason, the complete core layout including the transformers was exported for EM simulations in SONNET®. This is shown in Fig. 4.72. The complex nature of the circuit requires correct placement of ports at different points in the layout. Treating one end of the primary and secondary coil of each transformer as common-ground, the eight remaining ends are connected to eight different ports as shown in Fig. 4.73a. In order to verify the correctness of this setup, another simplified version reduces the number of ports to four as shown in Fig. 4.73b. After the time and memory consuming EM-simulations, the resulting s-parameters are exported to ADS for post-processing and comparison between the two setups as show in Fig. 4.74. The s-parameters of two equivalent ports are compared in Fig. 4.75 and the close match between the two setups confirms the correctness of the eight port complete setup. This is subsequently utilized to extract the primary and secondary inductance of the four transformers including interconnects between its terminals and transistors and, the DC lines surrounding them.

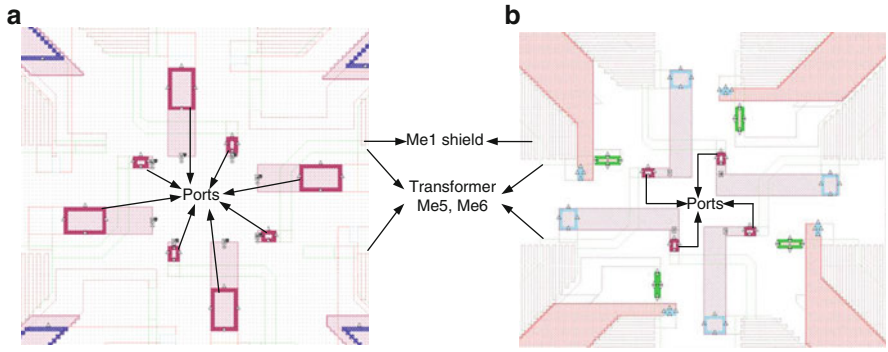

Fig. 4.73 Port placement using all eight ports (**a**), and simplified version using four ports (**b**)

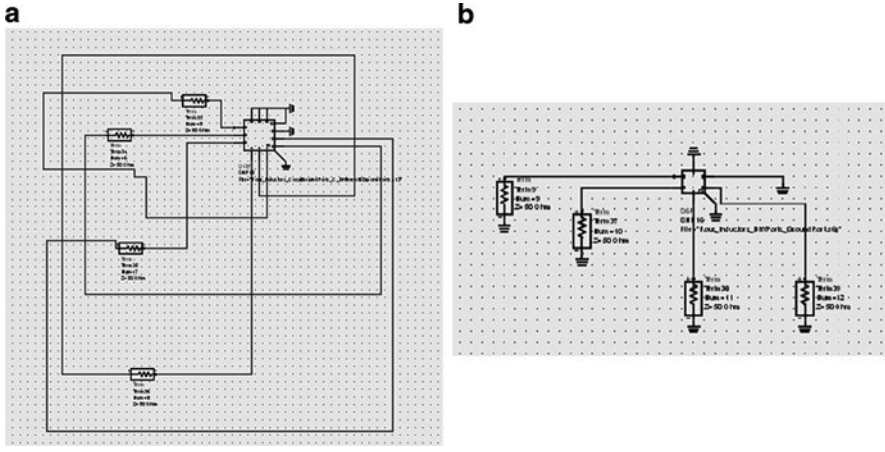

Fig. 4.74 ADS setup using EM simulated eight port block (**a**), and four port block for verification (**b**)

The impedance Smith-chart of the four transformers is plotted in Fig. 4.76 within a frequency range of 40–120 GHz. The secondary inductance of the four transformers matches closely. However, the primary coil (constructed by the top-metal) impedance is not identical for the four transformers and even behaves capacitively above a certain frequency for all four transformers. Furthermore, the quality factor of the coils is found to be ∼2 at 60 GHz which is much lower than the simulated Q-factor (∼17) of an individual transformer (discussed in the Section 4.1.5). This discrepancy between Q-factors is found to be the reason for the non-oscillatory behavior of the I-Q VCO.

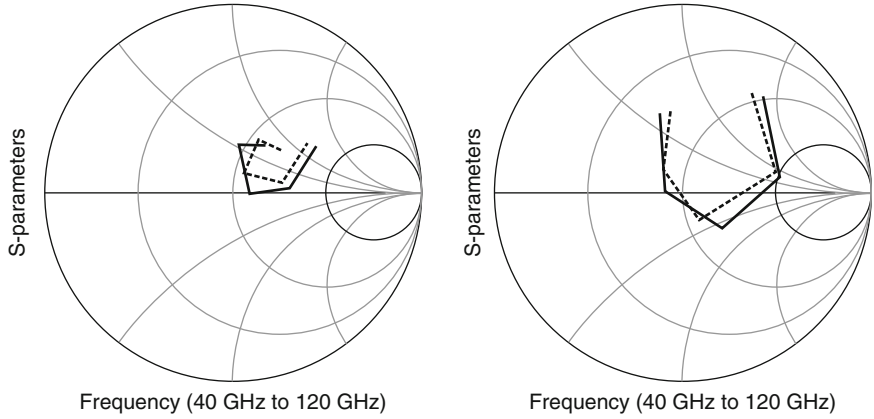

Fig. 4.75 S-parameters of the two setups for equivalent port numbers: Eight-port (*dashed*), four-port (*solid*)

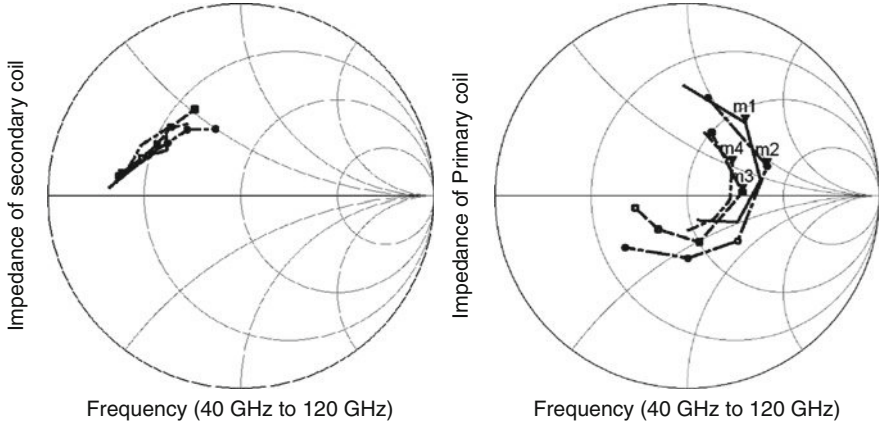

Fig. 4.76 Impedance of primary (*right*) and secondary coils (*left*) of the four transformers

4.2.6 Dual-Band VCO for 40 and 60 GHz

The preceding Sections 4.2.3–4.2.5 have presented individual 40 and 60 GHz VCOs. As in the case of a prescaler where the divide-by-2 and divide-by-3 function was merged in a dual-mode divider, the natural step forward for the above VCOs is to combine the two into one component. In other words, to design a multi-band VCO which could oscillate at 40 GHz as well as 60 GHz with the desired tuning

range of 10% in both bands. This section investigates the possibilities to achieve the above-mentioned task.

With the advent of many wireless standards operating at closely spaced frequencies, especially below 10 GHz, dual-band and multi-band VCOs has been a topic of intensive research in recent years. A large number of published works [121–130] have proposed different methods to achieve this dual-band operation. The most commonly adopted method involves modification in the frequency defining part of the oscillator which comprises the inductor(s) and the varactors. This is usually achieved by means of switches, which add/or subtract the effective inductance or capacitance from the tank yielding different oscillation frequencies [121, 122, 129]. The merits of this method for mm-wave frequencies will be discussed next.

The viability of "switch approach" for high frequency VCOs can be investigated by a simple example. In addition to the required 40 and 60 GHz bands, let us consider a dual-band VCO required for WLAN frequency bands at 2.5 and 5 GHz. Assuming nominal inductance values, the required capacitance for each frequency is shown in Table 4.4.

The capacitance values in case of WLAN are in the pico-farad range. This high capacitance value can easily incorporate the fixed capacitance introduced by the switch. Thus, capacitors for band-selection can be switched in or out from the tank and the required tuning can be provided by varactors. On the other hand, the total required capacitance for mm-wave VCOs is in the femto-farad range (as in VCO designs in the preceding sections). Furthermore, this includes the fixed capacitance from the transistors as well as the variable capacitance to achieve the desired tuning range. It is clear that adding a switch, will further reduce the tunable portion of the capacitance, resulting in a failure to achieve the tuning range. In order to gauge the fixed capacitance of a switch, Fig. 4.77 shows the increasing trend as a function of switch width in 65 nm CMOS technology. In case of a 60 GHz VCO, a 50 μm wide switch adds a fixed capacitance of 30 fF, which is 34% of the 87 fF total capacitance. Switching an inductor in and out of the tank for band-selection is another option, but it poses a similar dilemma. Ideally, the smallest width for the switch would be preferable to keep the added capacitance low; however this choice adds a considerable resistance in series with the inductor when the switch is ON. As shown in Fig. 4.77, for a 20 μm switch, the ON resistance is as high as 17 Ω and can severely affect the tank Q-factor. As a solution, the loss can be overcome by increasing the negative resistance of the oscillator, implying an increase in dimensions of the VCO transistors. An alternative is to increase the switch width itself which can decrease the ON-resistance within acceptable limits. However, both the

Table 4.4 Capacitance values for dual-band VCOs for WLAN and mm-wave frequencies

Frequency (GHz)	Inductance	Capacitance
2.5	2 nH	2 pF
5		0.5 pF
40	80 pH	198 fF
60		87 fF

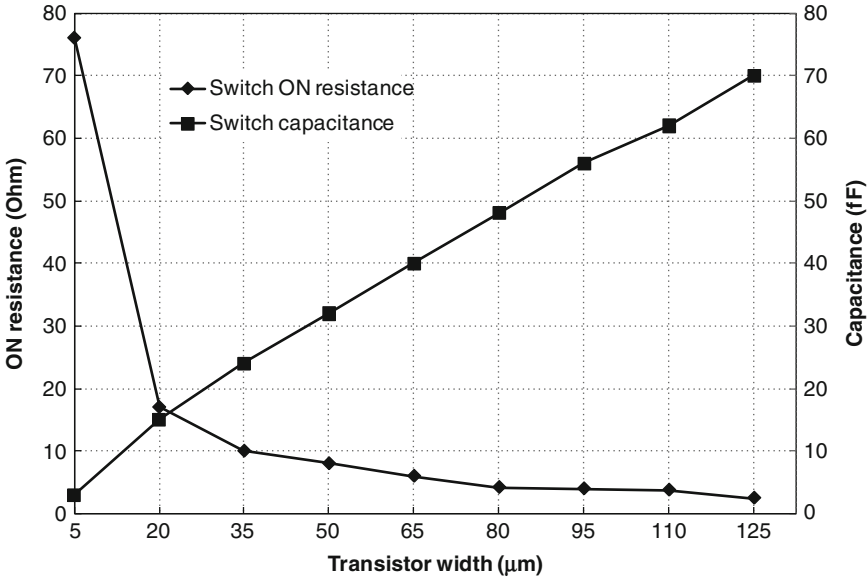

Fig. 4.77 Capacitance and ON resistance of a MOS switch as a function of width

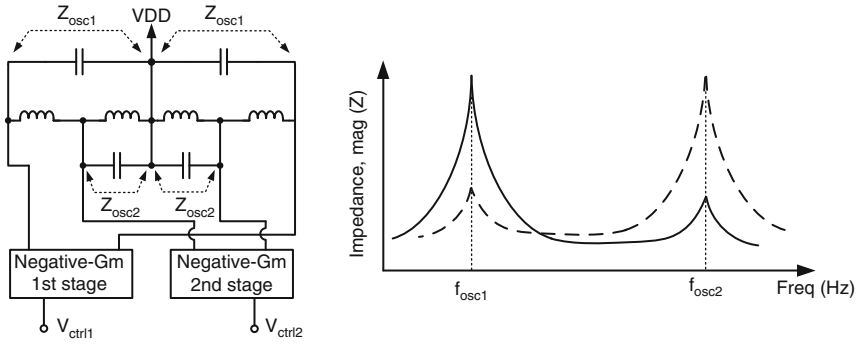

Fig. 4.78 A dual-band VCO approach based on fourth order resonator and the resulting oscillation frequencies

above solutions will again add significant fixed capacitance to the total tank capacitance resulting in reduction of tuning range. The above trade-offs indicate that the switch approach has serious shortcomings for mm-wave VCOs.

There are a number of other methods for achieving dual-band VCOs, the first of which make use of high order resonators or double-tuned transformers which demonstrate multiple oscillation modes [125, 126, 128, 129]. The oscillation frequencies are controlled by the connection of the negative-Gm stages. One such an example is shown in Fig. 4.78 [125] where two negative-Gm stages are

permanently connected to different parts of an LC circuit exhibiting two distinct resonance frequencies. The first negative-Gm stage is connected to the outer LC circuit having equivalent impedance Z_{osc1} whereas the second one is connected to the inner LC circuit with equivalent impedance Z_{osc2}. Due to a larger LC product for the first stage, the corresponding oscillation frequency f_{osc1} is lower than the second stage which has a higher oscillation frequency f_{osc2} due to smaller LC product. This is shown on the right hand side of Fig. 4.78. Although this method provides a dual-band solution without the need of switches, it poses a number of other problems. The first is the silicon-area penalty due to multiple inductors required to form the high order tank. Although at mm-wave frequencies, the size of the required inductors is small but their close proximity necessitates careful EM-analysis. Secondly, if the loop gain is higher than one for both stages, dual-tone oscillations might occur which are undesirable. Thus, in practice only one stage is enabled at a time by using control voltages (V_{ctrl1}, V_{ctrl2} shown in Fig. 4.78) which can be connected to nodes that are isolated from the tank so that the Q-factor remains unaffected. However, using this approach, the parasitic capacitances of the "switched-off" stage are added to the total capacitance, reducing the tuning range. As an example, the reported FTRs for a 0.8/1.8 GHz dual-band VCO in [125] are only 56 and 121 MHz, respectively.

Transformers can also be utilized for dual-band VCO operation. In this method, the primary or secondary coil is included or excluded from the circuit, resulting in a change in inductance and hence oscillation frequency. However, the off-state capacitance and complexity are two major drawbacks of this approach. Lastly, RF-MEMS switches offering low resistive losses have the potential to be used for switching inductors or capacitors; however, current IC technologies in general and the available CMOS 65nm in particular do not offer integration of such switches.

The above discussion implies that more investigation is required to achieve dual-band VCOs at mm-wave frequencies which along with the frequency separation, is able to provide the required tuning range. Therefore, the proposed synthesizer in this book utilizes two separate VCOs operating at 40 and 60 GHz, individually satisfying the tuning range and phase noise requirements.

4.3 Synthesizer Front-Ends

The design of individual components for the proposed synthesizer front-end provided valuable experience and insight into the bottle-necks for each component. The frequency shift observed during measurements as compared to simulations provided an estimate about the over-design required for subsequent designs. Furthermore, the use of varactors in the majority of VCO and ILFD circuits gave useful information about their tuning capabilities in real measurements. The accuracy of EM solvers was also verified by measuring a transformer test-structure (Section 4.1.5). The next natural step is the integration of the VCO and ILFD, forming the synthesizer front-end. Despite the above-mentioned insights gained

by individual component design, the integration of two high frequency blocks offers its own set of challenges and requires careful investigation. Therefore, this section discusses the integration of the 40 and 60 GHz front-ends for the proposed synthesizer.

4.3.1 40 GHz VCO and Divide-by-2 ILFD

Frequency synthesizers at frequencies below 10 GHz have the luxury to utilize broadband prescalers, such as the static frequency divider (Section 4.1.2). In such synthesizers, there is no issue of synchronization between the VCO and prescaler as the latter can easily cover the complete tuning range of the VCO. On the other hand in mm-wave synthesizers, like the one proposed in this work, the VCO (Section 4.1.3) as well as the prescaler (Section 4.2.3) are LC resonator based. Due to the frequency selectivity of these resonators the major challenge while integrating two such components is the synchronization of the tuning range of the VCO with the locking range of the ILFD. Any frequency mismatch due to design inaccuracy or layout parasitics can reduce the effective operation range of the synthesizer or, in worse case, make it completely devoid of locking. Therefore, it is important to integrate the front-end of the synthesizer prior to its complete integration including the back-end. The experience gained and frequency-shifts observed during individual components realization assist in achieving a synchronized front-end. This section includes the integration of the 40 GHz front-end as well as the modifications made in the VCO and ILFD based on their measured results.

The complete schematic of the synthesizer front-end is shown in Fig. 4.79. The 40 GHz VCO shown on the left hand side is a simplified version of the circuit presented in Section 4.2.3. The aim in this version is to maximize tuning range so that in case of any frequency shift the measured tuning range still covers the desired frequency band. The enhancement of tuning range can be achieved by decreasing the fixed capacitance part of the tank capacitance. This provides more "room" for the variable capacitance from the varactors whose C_{max}/C_{min} can be raised to achieve a wider tuning range. In order to reduce the fixed capacitance, a number of modifications are made. Firstly, an only-NMOS topology is chosen which removes the capacitance contribution from the PMOS devices present in a complementary structure. Secondly, the tuning circuit is simplified by removing the MIM capacitors because, despite the increase in the Q-factor due to their usage, they decrease the more important C_{max}/C_{min} ratio for this design. The tuning of the varactors is also done single-endedly as opposed to differential tuning in the earlier version. There are two reasons aiding this decision. Firstly, the phase noise of the measured VCO is better than the target specifications by 6 dB so the phase noise degradation due to single-ended tuning can be tolerated. Secondly, the final synthesizer circuit is to be measured on-wafer and due to limitation of DC-pads, single-ended tuning is used to save one such bond-pad.

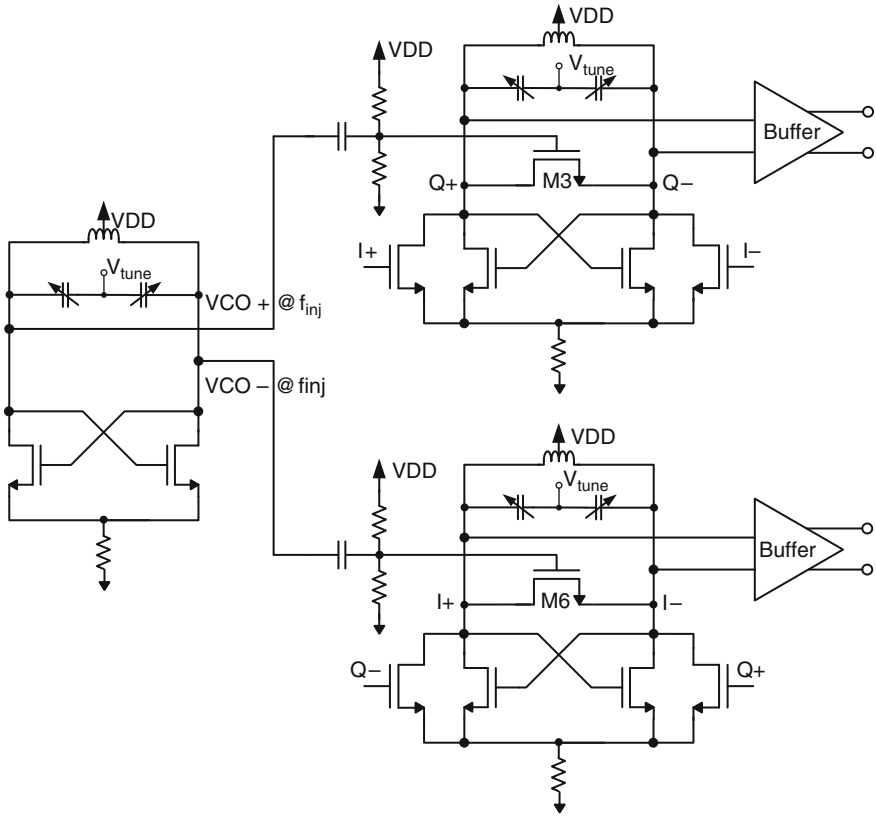

Fig. 4.79 Forty gigahertz synthesizer front-end

The VCO inductor, similar to the earlier version, is a single-turn top-metal inductor of 95 pH with a Q-factor of ∼20 at 40 GHz. Each varactor is composed of 30 multi-fingers, having a length and width of 300 nm and 2 μm per finger, respectively. The maximum and minimum capacitances are 106 and 30 fF resulting in a C_{max}/C_{min} ratio of 3.53. The Q-factor of the single-endedly tuned varactor setup is between 6 and 20, for a tuning voltage of 0–1.2 V. The NMOS transistors of the VCO are 1.5 times the earlier version, to generate enough negative resistance in the absence of the PMOS pair. The post-layout simulation of the VCO yields an FTR from 38 to 45 GHz. This 16% tuning range is double as compared to the earlier design. The VCO consumes 5 mA from a 1.2 V supply (1.6 times the earlier design). Due to the only-NMOS topology the output differential swing of the VCO is larger as compared to a complementary structure. The simulated peak-to-peak amplitude is about 1.5 V.

The quadrature injection locked frequency divider in Fig. 4.79 is identical to the stand-alone ILFD circuit presented in Section 4.1.3. The differential outputs of the

VCO are injected to the input transistors M3 and M6 present in the two separate stages of the ILFD. As the output swing of the VCO is sufficiently large, buffers are not required between the ILFD and VCO, which greatly simplifies the routing during layout and decreases the power consumption of the overall system. The injection transistor requires a different biasing voltage as compared to the DC-level of the VCO output, thus AC-coupling capacitors are used and the ILFD is biased independently. The value of the coupling capacitor is important as a capacitive divider is formed between the coupling capacitor and the gate-source capacitance of the injection transistor. If the former is chosen of the same order as the latter, part of the injection signal will be lost in the gate-source capacitance. Therefore, the coupling capacitor of 50 fF is chosen which is seven times the gate-source capacitance of 7 fF. At simulation level, some intentional loss is introduced in the injection signal to model the layout losses.

As discussed previously, the synchronization of the tuning range of the VCO and locking-range of the divider is of utmost important. Therefore, the varactor setups of both components are designed in a way that the FTR of the VCO coincides with double the free-running FTR of the ILFD. Thus, the tuning voltages (V_{tune}) of both components can be tied together for synchronized operation. This approach ensures that for each tuning voltage minimum power is required by the frequency divider for injection locking. In addition, for subsequent integration of the complete synthesizer the output of the loop-filter can be connected to both components for correct operation.

The chip micrograph of the 40 GHz front-end is shown in Fig. 4.80. The VCO, visible at the top, is placed as close as possible to the ILFD. All the transistors including VCO, ILFD and the output buffers are located in the encircled area. The buffered ILFD offers quadrature outputs but only one of these is measured and the other is terminated on-chip. The dimensions of the output transmission lines are similar to the one in Section 4.1.3. The total chip area is $700 \times 500\ \mu m^2$ where as the active core area occupies $80 \times 100\ \mu m^2$.

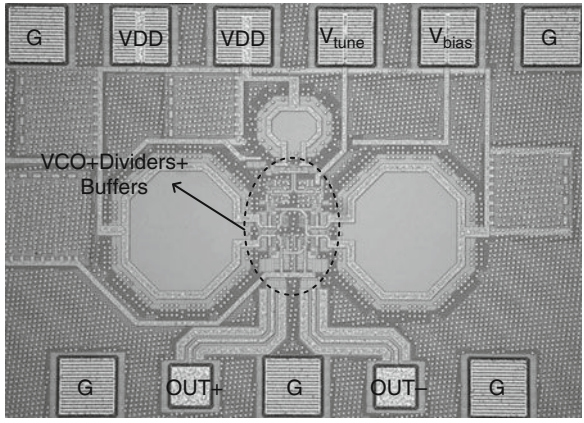

Fig. 4.80 Chip micrograph of 40 GHz synthesizer front-end

As the other circuits, the front-end is also measured on-wafer with the output from the ILFD observed on a spectrum analyzer. At first, the VCO is kept switched-off to measure the free-running frequency range of the ILFD. The tuning voltage is varied between 0 and 1.2 V yielding a similar free-running frequency as the stand-alone ILFD of Section 4.1.3. Shown in Fig. 4.81, the minimum and maximum values are 17.6 and 21 GHz. The VCO is then switched ON with a supply voltage of 1.2 V. At $V_{tune} = 0$, the output is observed to lock at 18.8 GHz, which implies that the VCO is oscillating at 37.6 GHz (400 MHz lower than the corresponding simulated frequency). The tuning voltage is then incremented and having a combined V_{tune} for both components, moves them towards higher frequency in a synchronized manner. At 0.6 V, a locked spectrum at 19.9 GHz and at the maximum V_{tune} of 1.2, a peak at 21.1 GHz is observed. Thus, the total locking range referred to the input of the ILFD is from 37.6 to 42.2 GHz. The measured operation range of the front-end is very close to the target range of 38–42.3 GHz. The locking is also observed for lower supply voltage of the VCO. However, as the output amplitude of injection signal decreases with the supply voltage, the locking range is correspondingly smaller. The DC-power consumption of the VCO and ILFD is 6 and 9 mW, respectively and the two common-source differential output buffers consume 12 mW.

The phase noise of the synthesizer front-end is measured in two situations. First, in the free-running state of the ILFD and second in the locked state. In the former case, the phase noise is expected to be higher than the locked state. Figure 4.82 shows the free-running and locked phase noise for a 19.9 GHz output frequency which falls in the center of the locking range. At 1 MHz offset the locked phase

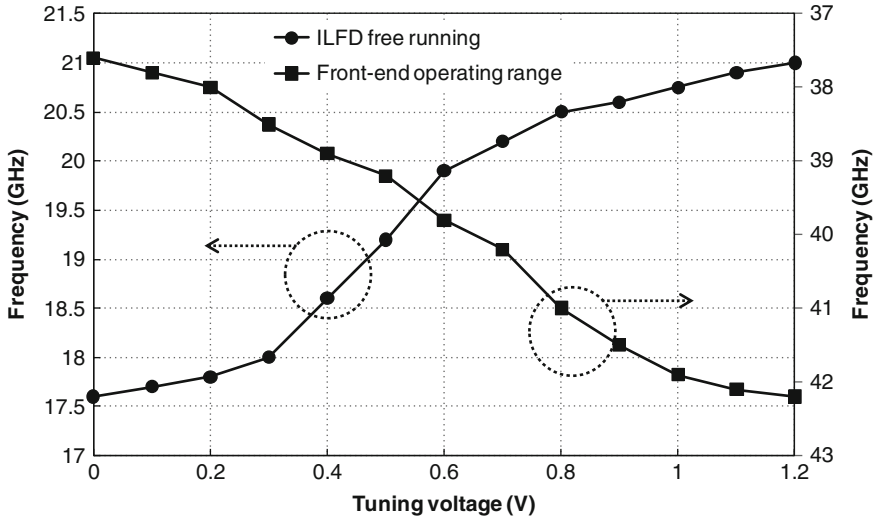

Fig. 4.81 Forty gigahertz synthesizer front-end operation range and ILFD free-running frequency

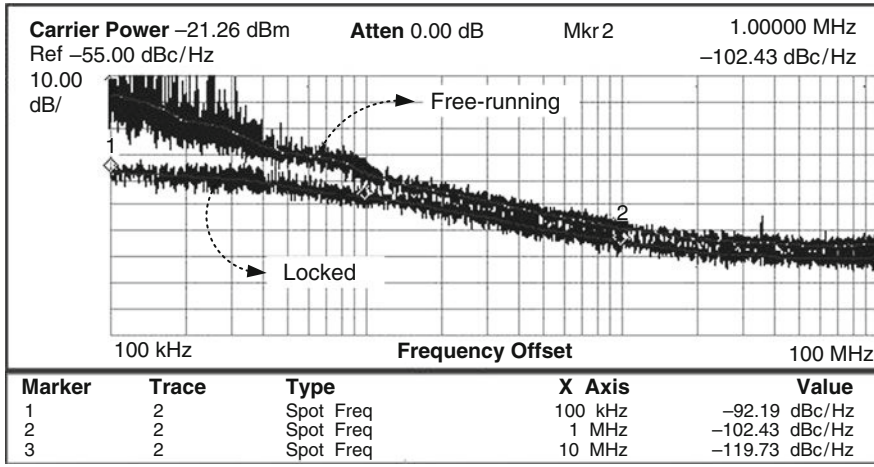

Fig. 4.82 Phase noise of the synthesizer front-end in free-running and locked state for a carrier frequency of 19.9 GHz

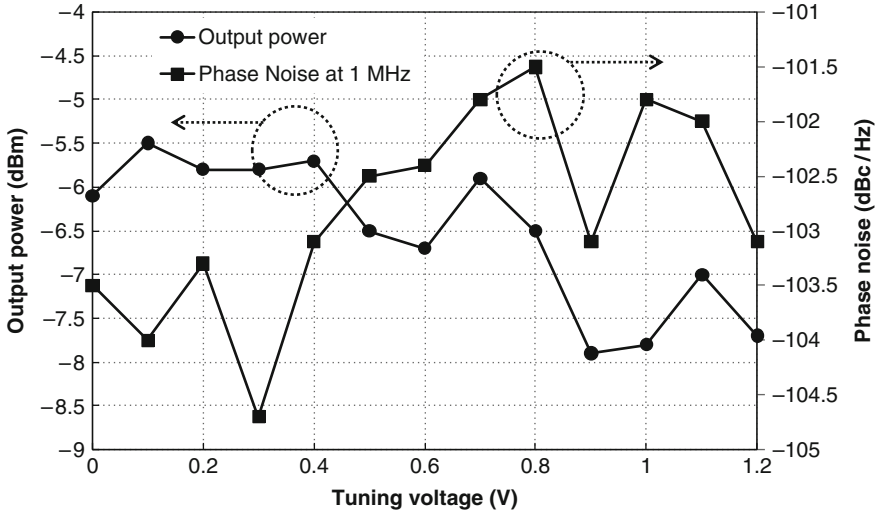

Fig. 4.83 Output power and phase noise variation for the 40 GHz synthesizer front-end

noise is 3.8 dB better than the free-running case whereas at lower offsets the difference is more profound. The variation of phase noise over the complete operation range of the front-end is ±3.2 dB. The output power, after de-embedding the losses of the cables and other measurement equipment lies between −5 and −8 dBm. The measured output power is an important parameter as the next divider stages in the synthesizer back-end need to operate correctly with this (or even lower) power level. The variation of phase noise and output power is shown in Fig. 4.83.

The phase noise performance of the synthesizer front-end is mainly dominated by the 40 GHz VCO. The individual VCO (of Section 4.2.3), although slightly different than the one used in the front-end, demonstrated a phase noise around −106 dBc/Hz at 1 MHz offset. Incorporating the difference due to frequency division implies a phase noise of ∼−100 dBc/Hz at the ILFD output. Thus, the measured phase noise between −101 and −104 dBc/Hz (Fig. 4.83), at the front-end output, confirms the dominating behavior of the VCO.

The integration of the 40 GHz synthesizer front-end is an important step towards complete system integration of the synthesizer. The measured results closely satisfy the target specifications; however, the output power might need to be boosted to some extent. This can be achieved by increasing the gain of the output buffers and will be revisited in Chapter 6 during the complete synthesizer integration.

4.3.2 60 GHz VCO and Divide-by-3 ILFD

This section discusses the 60 GHz front-end design which combines the 60 GHz I-Q VCO with a divide-by-3 ILFD to obtain the 20 GHz outputs similar to the 40 GHz front-end. The considerations for synchronization between the free-running FTR of the ILFD and the VCO FTR (now three times the ILFD frequency) are even more critical for a 60 GHz front-end as the parasitic effects are more dominant at this frequency.

The complete front-end schematic is depicted in Fig. 4.84. It combines the circuit schematics of the 60 GHz actively coupled I-Q VCO (of Section 4.2.4) and the dual-mode divider (of Section 4.1.6). The information gathered by design and measurements of these two components assists in extracting accurate simulation results from the transistor level design. The dual-mode ILFD is used in place of the single-mode divide-by-3 (of Section 4.1.4) because of its higher injection efficiency and larger locking range.[3] The measured free-running oscillation frequency of the ILFD was 16.8–19.2 GHz and the total locking range spanned from 48.5 to 59.5 GHz, which is lower than the required 57–63.6 GHz for the synthesizer front-end under consideration. Therefore, the free-running frequency in the current design was shifted upwards by reducing the tank inductor value to obtain a range from 19 to 21.5 GHz. The tuning voltage of the VCO and ILFD is tied together to enable a synchronized operation for both the components. The I-Q VCO design is also tweaked slightly. In the measured version, the VCO outputs were driving large buffer transistors, which is not the case in this design. The input injection transistors are comparatively smaller which reduces the fixed capacitance in the VCO LC-tank to some extent. This reduction is compensated by increasing the varactor capacitance to increase the C_{max}/C_{min} ratio. Thus, a 0.5 GHz increase in FTR is achieved

[3]The dual-mode ILFD can also be utilized in the 40 GHz front-end; however, due to time-constraints it was not implemented.

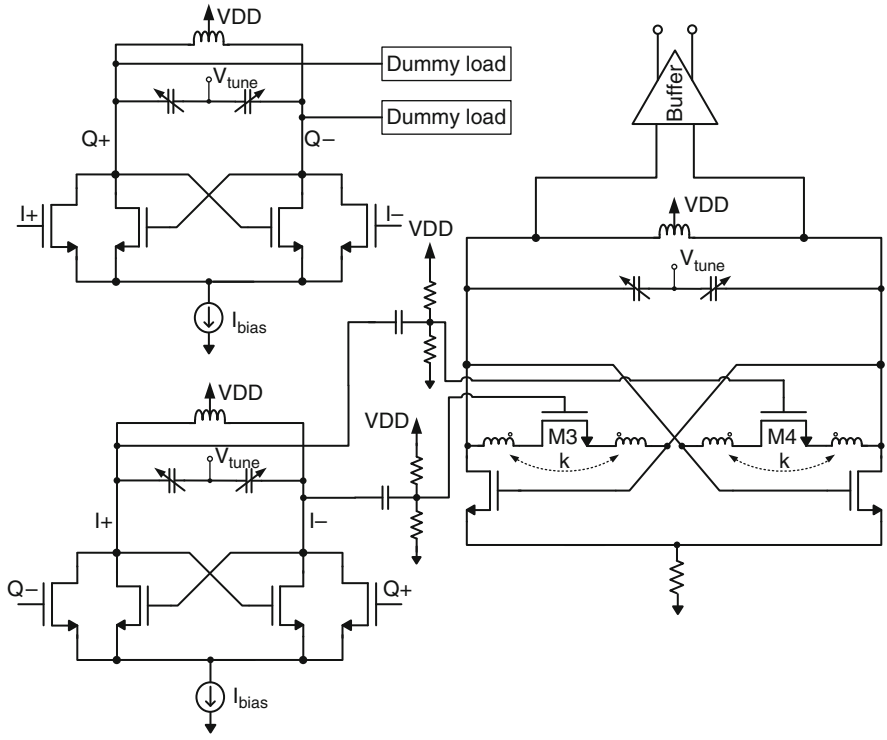

Fig. 4.84 Sixty gigahertz synthesizer front-end

which now spans from 57 to 63.5 GHz. One of the quadrature outputs is connected to the ILFD whereas the other is terminated in dummy loads which preserves symmetric loading for both I and Q outputs. The VCO is AC-coupled to the ILFD and separate biasing is used for the injection transistors.

The ILFD free-running frequency in the absence of the injection signal from the VCO is plot-ted in Fig. 4.85. Using a supply of 0.8 V, it consumes 5 mA as the previous design. The VCO is then switched on and for a biasing current of 10 mA and , the tuning voltage of the varactor is varied from 0 to 1.2 V. Both the VCO and ILFD move towards higher frequency in a synchronized manner as the same V_{tune} is utilized for both components. The operation range of the front-end is also plotted in Fig. 4.85 and is mainly determined by the VCO FTR. For higher values of Vtune (upto 1.5 V), the front-end still locks to the VCOs output which is higher than the shown maximum of 63.5 GHz. The phase noise of the synthesizer front-end is dominated by the VCO phase noise and the simulated values at 1 MHz offset for the locked front-end vary between −90 and −96 dBc/Hz over the complete operating range.

The specifications for the 60 GHz front-end are satisfied at simulation level. However, sufficient margin for frequency shifts cannot be achieved due to the limited FTR of the 60 GHz VCO for V_{tune} of 0–1.2V.

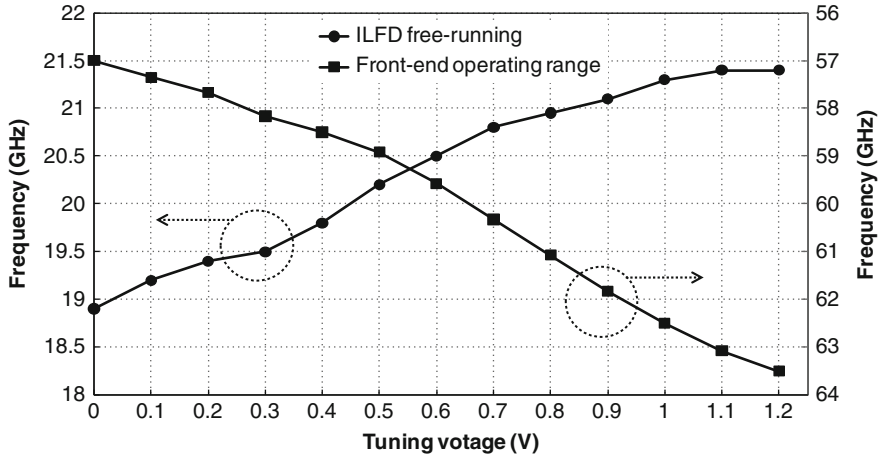

Fig. 4.85 Sixty gigahertz synthesizer front-end operation range and ILFD free-running frequency (simulated)

4.4 Conclusions

The design of a mm-wave synthesizer front-end, comprising a voltage controlled oscillator and prescaler, is without doubt the most challenging as compared to other parts of the synthesizer. This chapter has focused on the front-end components of the proposed synthesizer and presented a step-wise approach, starting with individual component design and ending at an integrated front-end.

An overview of different prescaler architectures, discussing their pros and cons is presented in Section 4.1.1. It is found that static and dynamic frequency dividers are easy to design and provide wide locking range but they fall short of reaching close to 60 GHz. Injection locked frequency dividers, on the other hand, can easily operate at mm-wave frequencies but their narrow-band nature results in smaller locking range. Thus, circuit design techniques have been adopted to improve the latter characteristic. Three examples of injection locked frequency dividers have been presented in Section 3.1. The 40 GHz divide-by-2 quadrature ILFD based on direct injection and input power matching, results in a 37% locking range. The 60 GHz divide-by-3 ILFD addresses the locking range issue by achieving harmonic enhancement through resistive feedback. This results in a 11% locking range. The last prescaler presented for the proposed synthesizer combines the divide-by-2 and divide-by-3 operations in one circuit, thus simplifying the overall system architecture considerably. The locking range for the dual-mode ILFD is 16.5% and 20.4% for divide-by-2 and divide-by-3 mode, respectively which satisfy the target specifications. For a proper comparison between ILFDs, two figure-of-merits are introduced in Section 4.1.7 which incorporate the use of varactor tuning as well as input sensitivity and DC power consumption.

The second major portion of this chapter is dedicated to the VCO which is the other important front-end component. An overview of various VCO architectures is presented among which LC-based VCOs are found to be suitable for high frequency operation and good phase noise. Three VCO circuits are presented next. The VCO for the 40 GHz front-end is a complementary cross-coupled structure and employs differential tuning for the capacitive tuning circuit. A measured FTR of 8.1% and a best phase noise of −106 dBc/Hz at 1 MHz is obtained. Two I-Q VCOs for the 60 GHz front-end are presented. The first is based on active coupling and demonstrates a FTR of 9.3% and phase noise of −95.3 dBc/Hz at 1 MHz offset. The second 60 GHz I-Q VCO is based on passive coupling using on-chip transformers. Operated at 0.8V, the VCO demonstrates a simulated FTR of 10% and a phase noise of −94 dBc/Hz. The transformer, measured as a separate test-structure, provides good agreement between EM simulations and measurements. An ideal solution for the proposed flexible synthesizer lies in a dual-band VCO which can operate at 40 as well as 60 GHz. However, the use of switches to move capacitors or inductors in and out of the tank is not found a prospective solution. This is because either the losses of the switch are too high, which degrades the tank Q-factor, or the fixed capacitance added to the tank is too large, which decreases the tuning range. Therefore, two separate VCOs operating at the aforementioned frequencies is a suitable way for synthesizer front-end integration.

The last section of this chapter presents the integrated synthesizer front-ends, which is an important step towards complete system integration. A modified and improved version of the 40 GHz VCO, in terms of FTR, is combined with the 40 GHz quadrature ILFD. The valuable experience gained during individual component integration assists in synchronizing the operation range of the two components fairly accurately. The operation range of the 40 GHz front-end is between 37.6 and 42.2 GHz and the best phase noise of −104.5 dBc/Hz is measured. Similarly, the 60 GHz front-end is formed by combining the corresponding actively coupled I-Q VCO and the dual-mode ILFD of Section 4.1.6. Based on the measured results of the dual-mode ILFD, its operation frequency is increased to match the FTR of the VCO. Subsequent simulations of the 60 GHz front-end satisfy the operation range and phase noise requirements.

Chapter 5
Design of Low Frequency Components

Abstract This chapter presents the PLL back-end circuits including the feedback divider chain, phase-frequency detector, charge pump and loop filter. Two approaches for feedback division are included; one based on cascaded CML frequency dividers and the second using a down-conversion mixer.

Keywords Phase frequency detector · Loop filter · Charge pump

The synthesizer components, apart from the VCO and prescaler, operate at lower frequencies in comparison with the synthesizer front-end. In this book, these components are collectively termed as the synthesizer back-end. In general, the back-end consists of a divider-chain, connected to the prescaler converting its output to a lower frequency where it can be compared to the phase-frequency detector. The PFD generates output pulses which control current sources in a charge-pump, thus converting the phase and frequency difference between the divided feedback signal and the reference frequency to current pulses. These pulses are then converted to a voltage and after passing through a low-pass filter, utilized for tuning the voltage controlled oscillator to the appropriate frequency. The design of the back-end poses a different set of challenges in comparison with the front-end. In the latter, high operation frequency, wide tuning and locking range requirements, coupled with profound effects of parasitics were the major bottlenecks. On the other hand, the synthesizer back-end entails challenges such as precision and matching in PFD and charge-pump, large power consumption of feedback divider chain and integration of the loop filter. This chapter discusses the design and implementation of the synthesizer back-end and the underlying components.

The highlighted synthesizer back-end is shown in Fig. 5.1. The frequency division (or conversion) of the prescaler outputs is discussed in Section 5.1. Two methods to achieve this are presented. First is the conventional approach using a cascade of frequency dividers and the second is based on a mixer. The remaining components of the back-end namely, phase-frequency detector, charge-pump and loop-filter are covered in Section 5.2.

H.M. Cheema et al., *60-GHz CMOS Phase-Locked Loops*,
DOI 10.1007/978-90-481-9280-9_5,

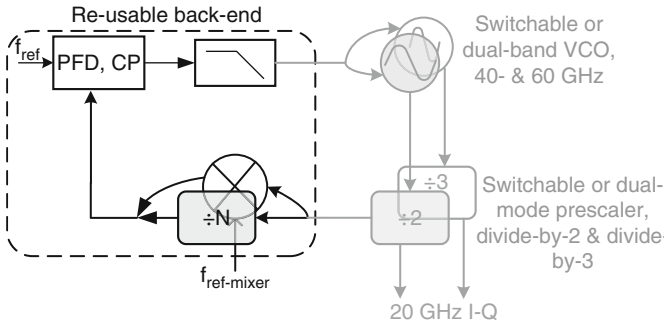

Fig. 5.1 Highlighted synthesizer back-end components

5.1 Feedback Division

The task of the divider chain (or mixer) after the prescaler is to generate an output which is very close to the reference frequency of the synthesizer. In this work, the prescaler output frequency is in the vicinity of 20 GHz whereas the reference frequency is 300 MHz. A simple method to achieve this task is to cascade a number of divider stages each having a division ratio of 2 or higher. The latter is an attractive choice as the frequency translation can be achieved with fewer stages. However, as the division ratio increases the locking ranges as well as the operation frequencies tend to decrease which can be a potential bottleneck. This will be discussed in Section 5.1.1. Another option investigated in this work is to down-convert the output of the prescaler directly to the PFD frequency by employing a mixer. Evidently, this method alleviates the requirement of multiple frequency division stages. However, it requires a fixed LO signal for the down-conversion. This approach will be elaborated further in Section 5.1.2.

5.1.1 CML Based Divider Chain

The divider chain is an important part of the synthesizer as it can be used to control the overall division ratio of the synthesizer. The distinct output frequencies or the number of channels to be supported by the synthesizer dictates the required division ratios. A mechanism to change the division ratio from one value to another in the feedback divider chain directs the synthesizer to jump from one frequency to another. This is generally achieved by implementing a dual-modulus (or multi-modulus) frequency divider (DM-FD) in the feedback loop.

A DM-FD is essentially a divider whose division ratio can be switched from one value to another by an external control signal. If such a divider is combined with a number of fixed division ratio dividers, a range of division ratios is obtained. For instance division ratio of a large number like 32/33 can be obtained by combining

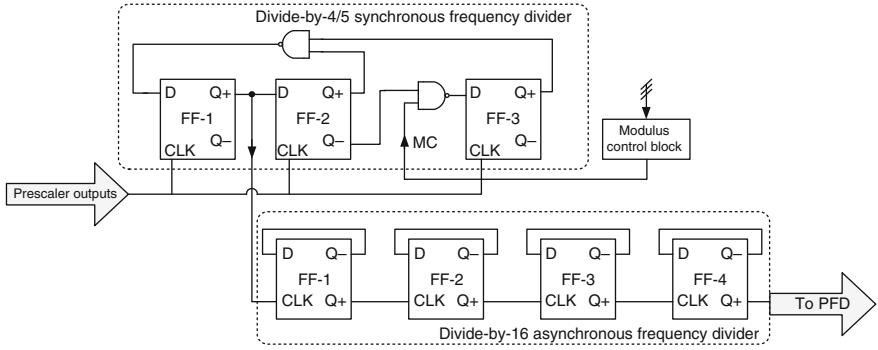

Fig. 5.2 Combination of a synchronous 4/5 divider and a divide-by-16 asynchronous divider to obtain multiple division ratios

a synchronous DM-FD with smaller numbers (such as 2/3 or 4/5) followed by a specific number of asynchronous dividers. Similarly, higher modulus dividers can be designed by controlling the operation of the synchronous DM-FD. This will be explained shortly. Recalling the synthesizer frequency plan presented in Section 2.4.2, the total required division ratio for the 40 GHz front-end and 500 MHz channelization is 127–142. Due to the use of divide-by-2 ILFD as prescaler, the required division ratios after this component are also reduced by half, i.e. 63.5–71. If the first division ratio is rounded-off to 64 for simplicity, the required division ratios become 64–71. One way of obtaining these division ratios is shown in Fig. 5.2 and is discussed next.

The circuit consists of three main blocks: a divide by 4/5 synchronous frequency divider, divide-by-16 asynchronous divider and a modulus control block. The divide-by-4/5 circuit consists of three D-flip-flops and two NAND gates. The first two flip-flops (FF-1 and FF-2) form a divide-by-4 circuit and in order to obtain the divide-by-5 operation, a third flip-flop (FF-3) is added and controlled by a NAND gate at its input. Thus, it can included or excluded from the circuit based on the NAND gates inputs, one of which is the modulus-control (MC) coming from its corresponding block. The divide-by-16 asynchronous divider is a series of divide-by-2 circuits formed by D-flip-flops. The prescaler (ILFD) outputs at 20 GHz are provided to the synchronous 4/5 divider which after proper division transfers its first flip-flop (FF-1) output to the asynchronous divider. The latter divides the signal by a fixed value of 16 and provides it to the phase frequency detector.

To understand the operation, it can be noted that when MC is high the synchronous divider divides by 4, whereas when MC is low an extra clock period delay is added by the third flip-flop resulting in a divide-by-5 operation. Thus, the modulus control block controls the number of times the synchronous divider is supposed to divide-by-5 over a certain time period. This characteristic can be exploited by using more than one bit for the modulus-control (MC). For instance, using a 3-bit control word (as in Fig. 5.2), the number of divide-by-5 operations can have eight different values and thus correspond to eight different division ratios for the overall circuit.

In the above case, a 3-bit control word can generate division ratios from 64 to 72, thus satisfying the requirement.

The synchronous 4/5 divider deals with the highest frequency in the above circuit coming from the ILFD outputs. Therefore, it is the most important part of the feedback divider. The highest operation frequency of the synchronous 4/5 divider depends on the propagation delay through its flip-flops and NAND gates, and to reduce this delay a number of improvements are employed. Firstly, as the outputs of the ILFD are differential, completely differential resistively-loaded CML based flip-flops are utilized (Section 4.1.3). Owing to smaller signal swings, this logic also enhances the operation frequency. Secondly, the NAND gates are merged [69] with the flip-flops to further reduce the propagation delay. Thirdly, to balance the loading of the three flip-flops, the input for the asynchronous divider is provided by the first flip-flop (FF-1) as the second flip-flop (FF-2) drives the third as well as the first flip-flop. As proposed in [69], the operation frequency can be increased and power consumption can be decreased considerably by reducing the transistor sizes and modestly increasing the load resistor values. This is in contrast with the approach of using large transistors and small load resistance, which results in high power consumption [131, 132]. Utilizing these techniques for improvement in operation frequency, the flip-flops, FF-1(similar to FF-3) and FF-2, are shown in Fig. 5.3.

The second flip-flop (FF-2) is made by two standard D-latches. The current sources in the tail-nodes are omitted to gain some voltage head-room. The first

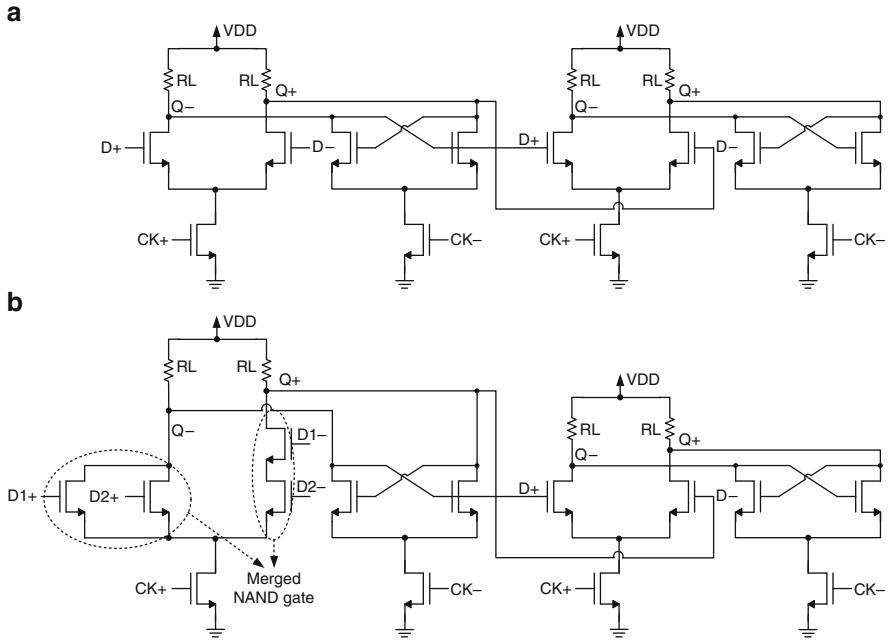

Fig. 5.3 Improved flip-flops for the synchronous 4/5 divider: FF-2 (**a**), and FF-1 (similar to FF-3) with merged NAND gate (**b**)

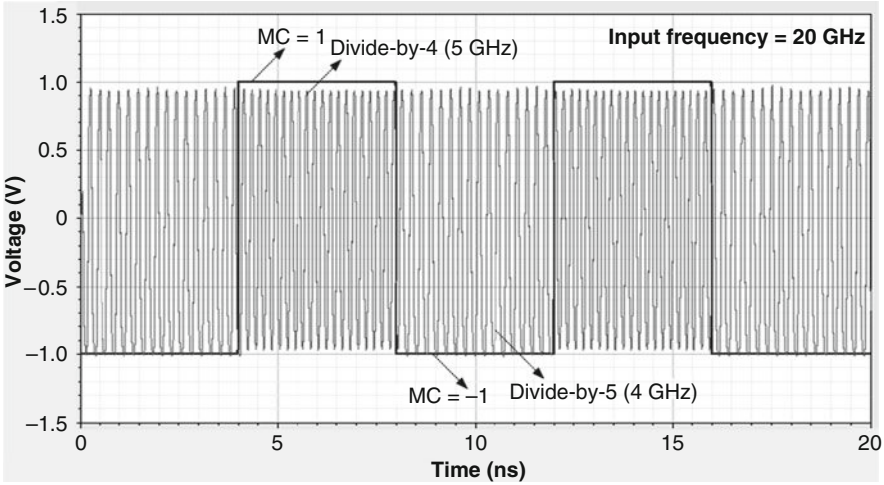

Fig. 5.4 Synchronous divide-by-4/5 simulated output for an input frequency of 20 GHz

flip-flop (FF-1) containing the merged NAND gate and D-flip-flop is shown in Fig. 5.3b. The first latch of this flip-flop contains four NMOS transistors to incorporate the NAND logic. The third flip-flop (FF-3) also includes a similar D-latch. Due to the differential structure of the D-latch and NAND gate, the required MC also needs to be differential. As mentioned previously, to reduce power consumption while maintaining a high operation frequency, the transistor dimensions are reduced and load resistance is increased. The optimized value of the load resistance (based on simulations) is 1.3 kΩ whereas the differential and cross-coupled pairs have widths of 2 and 1.2 μm respectively. The input clock transistors are 6 μm and the NAND gate transistors are 2 μm wide.

The transistor level simulations of the synchronous 4/5 divider are carried out in Cadence™ with CMOS 65nm technology. The variation of division ratio between 4 and 5 is observed by changing the MC voltage. For an input frequency of 20 GHz, the output of FF-1 is shown in Fig. 5.4. If the MC = 1, divide-by-4 operation results in an output frequency of 5 GHz, whereas for an MC = −1, the divider operates in the divide-by-5 mode resulting in an output frequency of 4 GHz. The highest operation frequency achieved for the synchronous divider is 23 GHz which covers the required frequency range of 19–21.15 GHz. The total power consumption of the synchronous divider is only 5 mA from a 1.2 V supply.

The modulus control block of Fig. 5.2 based on the three bit input word and additional control logic generates a pulsed MC signal to control the number of divide-by-5 operations of the synchronous divide-by-4/5 circuit. This block requires particular digital building blocks such as comparator and traditional CMOS NAND gates. Unfortunately, at the time of design the technology under use did not offer these ready-made blocks (with associated layout). Furthermore, the time limitation before the expected tape-out prevented custom design of the

modulus control block. Therefore, an alternate method for verifying the synthesizer operation and proof of concept was adopted. Recalling (2.3), the output frequency of the synthesizer is a product of the reference frequency and the combined division ratio including the prescaler (ILFD) and the subsequent divider chain. In the case, where the division ratio (N $\times$ P) is fixed, the output frequency can be varied by changing the reference frequency. This option was assisted by the fact that a clean external signal source was to be used for the proposed synthesizer and can be varied, if required.

The above-mentioned alternative simplifies the feedback divider chain which now can be a cascade of fixed divider stages. To obtain the output frequencies enlisted in Table 2.2 with a fixed overall division ratio of 128, the required reference frequency varies from 297.65 to 330.46 MHz. At the synthesizer output, this corresponds to frequencies of 38.1 and 42.3 GHz, respectively. Use of the ILFD as prescaler, reduces the required division ratio to 64 which is achieved by cascading six divide-by-2 stages ($2^6 = 64$) in series with each other.

The divide-by-64 cascaded divider is shown in Fig. 5.5. The prescaler (ILFD) outputs around 20 GHz are provided to the first divider stage which divides the frequency by 2 and passes it on to the second divider stage. The signal after going

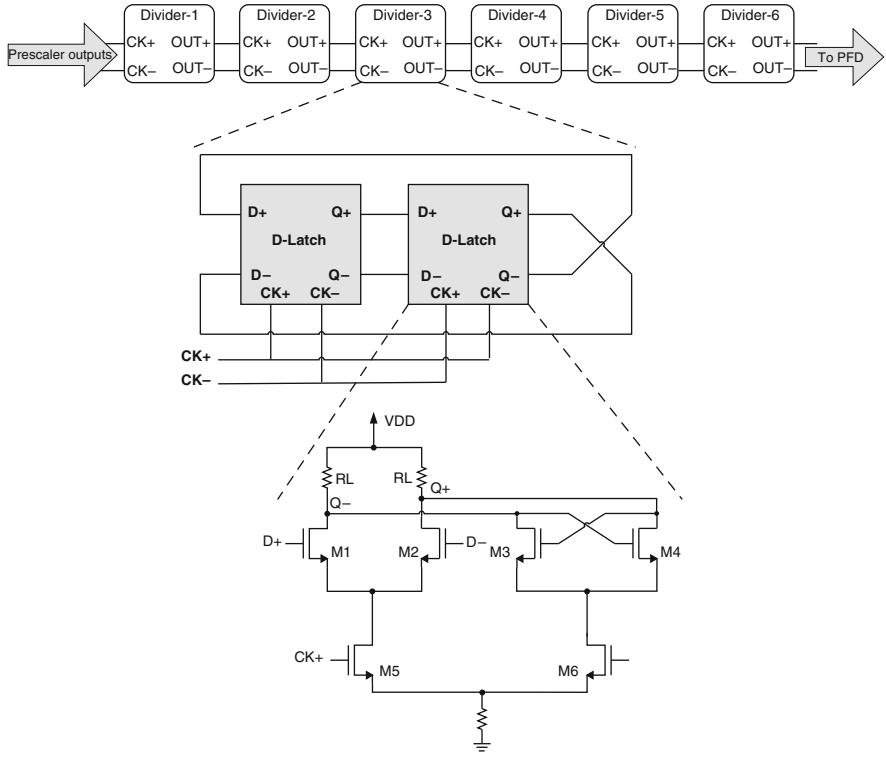

Fig. 5.5 Feedback divider chain, each divider is a flip-flop based on CML D-latches

Table 5.1 Current and power consumption of the feedback divider chain and individual stages

Frequency divider stage	Current consumption (mA)	Power consumption (mW)
1	1.38	1.66
2	0.83	1.00
3	0.75	0.90
4	0.71	0.85
5	0.64	0.77
6	0.68	0.82
Total	4.99	5.99

through six divide-by-2 operations is provided to the phase frequency divider by the last stage (Divider-6 on the right hand side). Each divide-by-2 stage consists of two D-latches in feedback, similar to the SFD presented in Section 4.1.2. Also depicted in Fig. 5.5, is the circuit schematic of each D-latch. The method adopted in the synchronous 4/5 divider to reduce power consumption while maintaining a high operation frequency is also employed for each frequency divider stage. The load resistors are moderately increased and transistor dimensions are decreased to obtain minimum power consumption. Each division stage is optimized independently based on its input frequency and the required operating range. Furthermore, the inputs and outputs of a particular stage are loaded with another divider circuit during the optimization process. Using a supply voltage of 1.2 V, the current and power consumption of the divider chain and each stage is shown in Table 5.1. The current gradually decreases as the operation frequency through the chain is decreased. The first divider stage consumes 1.38 mA as compared to 0.68 mA consumed by the last stage. The total current and power consumption for the complete chain is 5 mA and 6 mW, respectively. The divider chain covers the required operation range of 19–21.15 GHz with some margin for PVT variations. An example of the divide-by-64 operation is shown in Fig. 5.6. An input signal at 21 GHz, with an amplitude of 150 mV is used as an input to the divider chain. The latter is in accordance with the amplitude obtained from the 40 GHz front-end (Section 4.3.1). The divided output of 328.4 MHz is visible in the bottom graph of Fig. 5.6.

5.1.2 Mixer Based Division

The second method for frequency translation from 20 GHz at the prescaler output to ∼300 MHz at the PFD input involves the use of a mixer. This approach alleviates the requirement of a series of cascaded dividers and down-converts the frequency in one step. The evident advantage is the simplicity and a far less number of transistors as compared to the first approach. Furthermore, as the divider chain is a sequential circuit there is a delay contributed by each stage which adds to the settling time of the synthesizer. In the mixer based approach, the instant

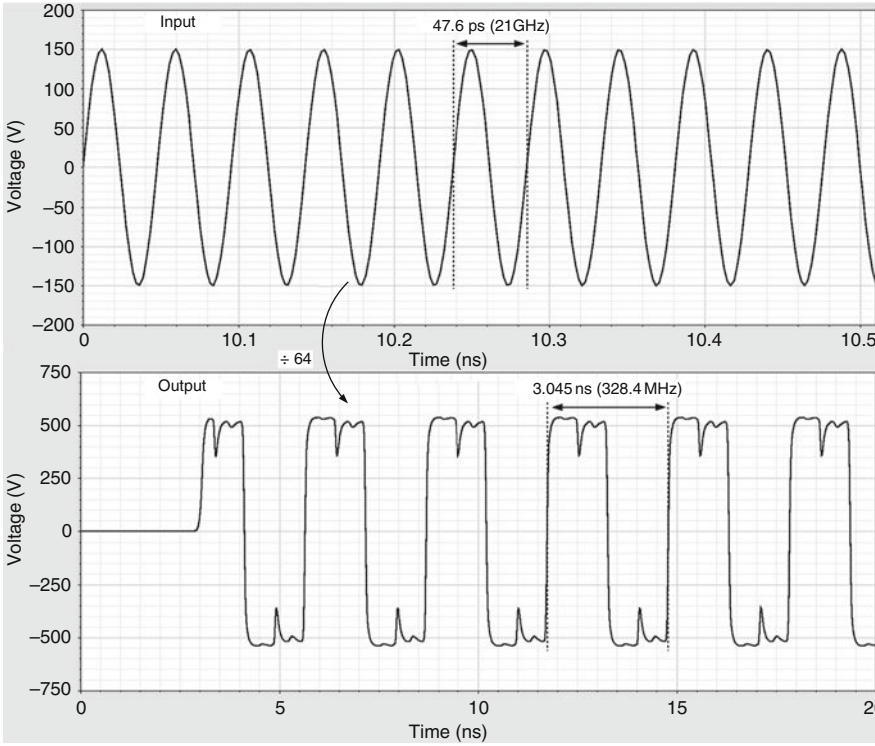

Fig. 5.6 Divide-by-64 operation for an input frequency of 21 GHz

conversion of frequency can reduce the settling time of the synthesizer (a comparison of settling time based on the two approaches will be presented in Chapter 6). The down-side of this approach is the requirement of a fixed LO signal which is an overhead for the synthesizer. However, as the required LO frequency is 20 GHz, ring oscillators can be utilized which consume small silicon-area in comparison to LC oscillators.

In order to further investigate the mixer based approach, a single-balanced mixer shown in Fig. 5.7 is analyzed. The RF input of the mixer is obtained from the prescaler outputs which can be a frequency anywhere between 19 and 21.15 GHz, whereas the LO signal is selected in a way that the steady-state down-converted frequency is always equal to the selected reference frequency. One such example is shown in Fig. 5.8 where the RF input is 20.32 GHz (top graph) and the LO is placed at 20 GHz. The resulting IF frequency is 320.5 MHz shown in the bottom graph. As the PFD commonly operates on square-pulses, the sinusoidal output of the mixer is converted into square pulses as shown in the bottom graph of Fig. 5.8 (discussed further in Chapter 6). The mixer is able to operate over the required RF frequency range of 19–21.15 GHz. The power consumption of the mixer is only 0.6 mW from a 1 V supply, which is 5.4 mW lower than the complete divider chain consumption

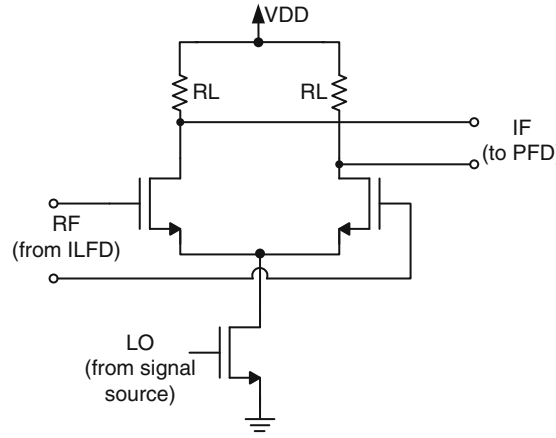

Fig. 5.7 Single-balanced mixer for feedback division

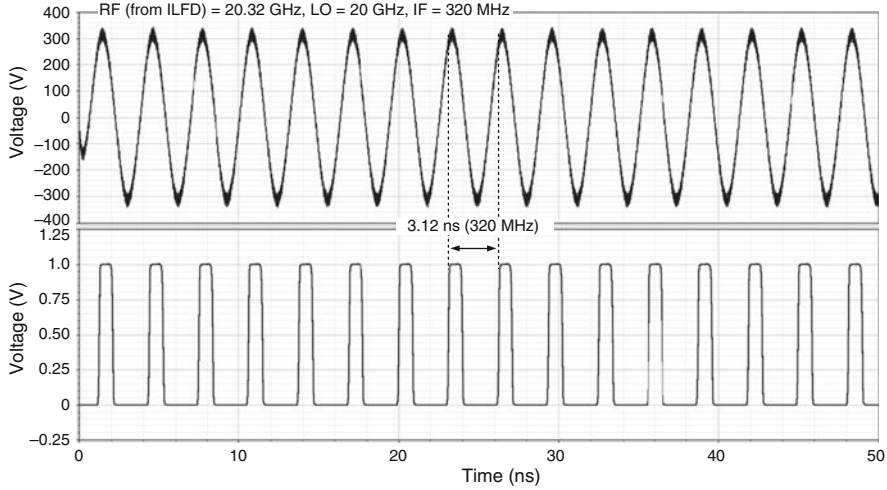

Fig. 5.8 IF output of the 20 GHz mixer, RF = 20.32 GHz and LO = 20 GHz

(Table 5.1). Thus, a clear advantage in power consumption is visible using the mixer based approach.

This section has presented two methods for achieving frequency division of the ILFD outputs to a lower frequency at which it can be compared to a reference frequency in the phase frequency detector. The first is based on a cascade of six divide-by-2 stages providing a division ratio of 64 whereas the second method is based on a single-balanced mixer which down-converts the frequency directly to ∼300 MHz. In Chapter 6, both these frequency division methods will be considered during complete synthesizer integration and their performance will be compared.

5.2 Phase-Frequency Detector, Charge-Pump and Loop Filter

This section discusses the remaining components of the synthesizer back-end, namely phase-frequency detector, charge-pump and loop filter. The combined task of these three blocks is to provide a stable DC tuning voltage to the VCO, based on the frequency (and phase) difference between the reference frequency and the output of the feedback divider chain so that the synthesizer can move towards lock. The role of each above-mentioned component will be elaborated in this section and their implementation for the proposed synthesizer will be presented.

The phase-frequency detector, as the name suggests, is a circuit which can detect both phase and frequency difference between two signals and generate an output representing that difference. A simple implementation matching the above characteristic is shown in Fig. 5.9a. It consists of two edge-triggered resettable D-flip-flops with their D inputs connected to logic ONE. In such a case the output of the flip-flop follows the clock input. The reference frequency (f_{ref}) and the output of the feedback divider chain (f_{div}) form the two inputs of the flip-flops. The operating principle of the PFD can be understood by a timing waveform shown in Fig. 5.9b. Assuming that f_{ref} leads f_{div} , a rising edge of the former causes the corresponding output UP to go high. Similarly, the rising edge of f_{div} triggers its output DN to go high. At this point, the AND gate becomes active and resets both the flip-flops until the next rising edge of either input arrives. Thus the phase-lead of the reference frequency manifests itself in proportional UP waveforms. Similarly, if the frequency of one of the inputs is different from the other, the resulting UP and DN pulses will have varying widths and will reflect that difference accordingly.

The PFD implementation of Fig. 5.9a poses a potential problem for small phase difference between the two inputs. In such a case a positive transition at UP (or DN) is closely followed by a reset operation. Due to the finite rise and fall times of the output pulses, it is possible that the UP and DN maybe pulled to low by this reset

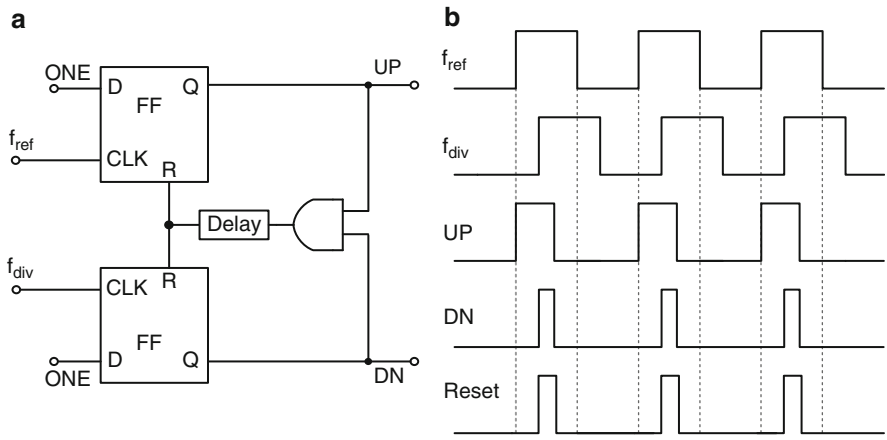

Fig. 5.9 PFD implementation (**a**), and its operating principle (**b**)

operation before they complete a positive (or negative) transition. Consequently, the UP and DN pulses cannot operate the charge-pump correctly. This region where the PFD is unable to track the small phase differences between its inputs is called "dead-zone". In a synthesizer, the presence of a dead-zone means that until the phase difference reaches a certain value, the loop fails to correct the error and the VCO control voltage does not change as desired. In other words, the loop is essentially open and the oscillator noise appears at the synthesizer output without being suppressed. A solution widely adopted to counter the dead-zone is to insert an intentional delay in the reset path. In practice, this is achieved by using a number of inverter stages after the reset NAND gate. This allows the PFD outputs UP and DN to complete their transitions before being reset to zero.

The basic PFD shown in Fig. 5.9a consists of D-flip-flops. The implementation of the latter, being an extensively studied topic leads to many PFD designs employing modified flip-flops or latches constituting these flip-flops [133–138]. The aim of these designs is generally to improve the characteristics of the PFD such as operation frequency, dead-zone, complexity, symmetry and robustness. In this work customized NAND gates are used to form the D-flip-flops and inverters. The gate level PFD implementation is shown in Fig. 5.10. The delay in the reset

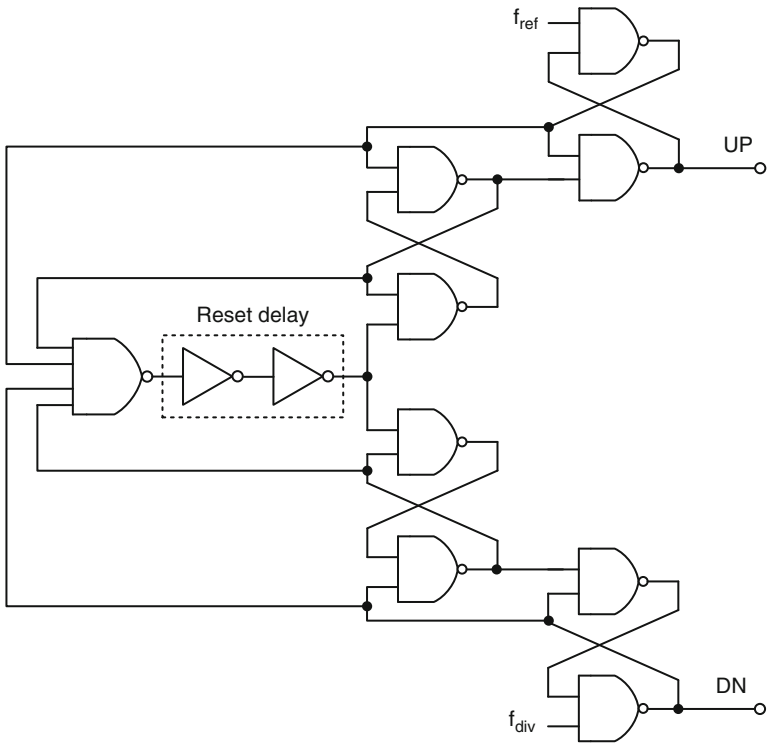

Fig. 5.10 Gate-level schematic of PFD

path is implemented by using two inverters which ensures the output pulses reach an amplitude, sufficient to turn-ON (or turn-OFF) the charge-pump. Thus the dead-zone is eliminated and is confirmed by simulations. An operation example of the implemented PFD is illustrated in Fig. 5.11. The reference frequency is set to 300 MHz whereas the other input, emulating f_{div}, is delayed by 600 ps and has a frequency of 328.4 MHz. As the latter has a higher frequency than f_{ref}, the corresponding PFD output DN has more pulses than UP. Thus, it will direct the charge-pump in a way to reduce the output frequency of the synthesizer and bring f_{div} closer to f_{ref}. The generated reset pulses can also be seen in response to both outputs UP and DN going high.

The next component in the synthesizer back-end is the charge-pump. Connected to the outputs of the PFD, it is responsible to pump-in or pump-out charge from the loop-filter and thus, moving the VCO control voltage up or down to initiate lock. Despite many variations in implementations, a charge-pump will invariably consist of two current sources and two switches. The operation of the charge-pump is illustrated in Fig. 5.12. The current sources provide a current of I_{UP} (or I_{DN}) which is diverted to (or from) the loop filter with the help of two PMOS and NMOS switches which are controlled by UP and DN pulses from the PFD. If, for example f_{div} is higher than f_{ref} (Fig. 5.11), the DN pulses will close the NMOS switch more frequently, dumping-out charge from the loop filter. This will decrease V_{tune} and the synthesizer output frequency, bringing the two frequencies closer to each other. The PMOS switch is usually controlled by an inverted version of the UP signal to maintain correct control polarity.

The main consideration for charge-pump design is matching the up (I_{UP}) and down current (I_{DN}). Any mismatch between the two results in a net charge deposited onto the loop filter at every comparison cycle. Thus, there is a periodic ripple on

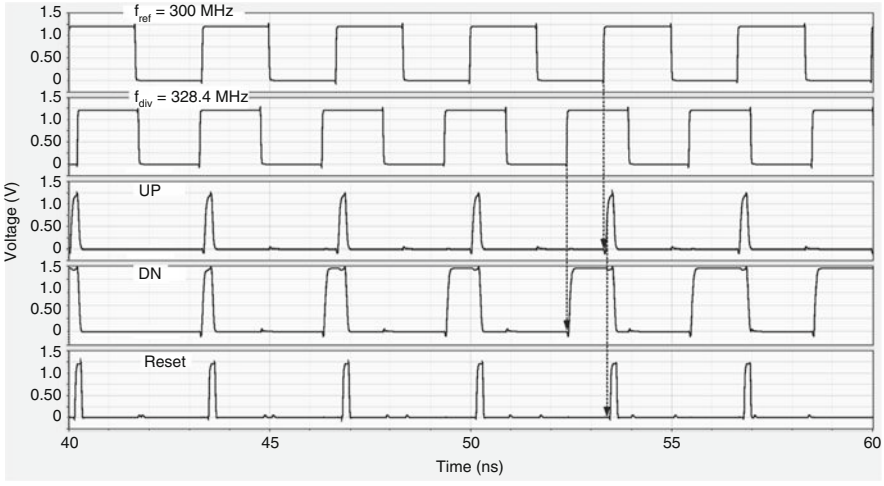

Fig. 5.11 Phase-frequency detector outputs for $f_{ref} = 300$ MHz and $f_{div} = 328.4$ MHz

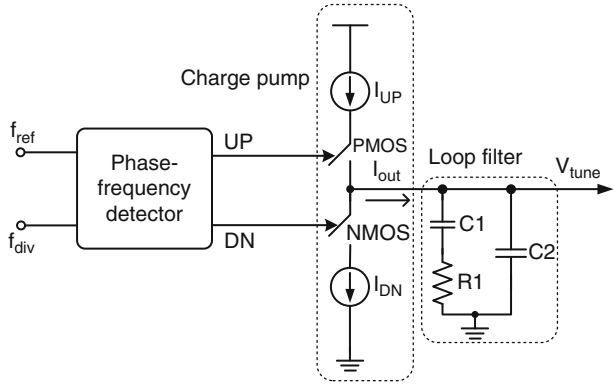

Fig. 5.12 Charge-pump principle in combination with PFD and loop filter

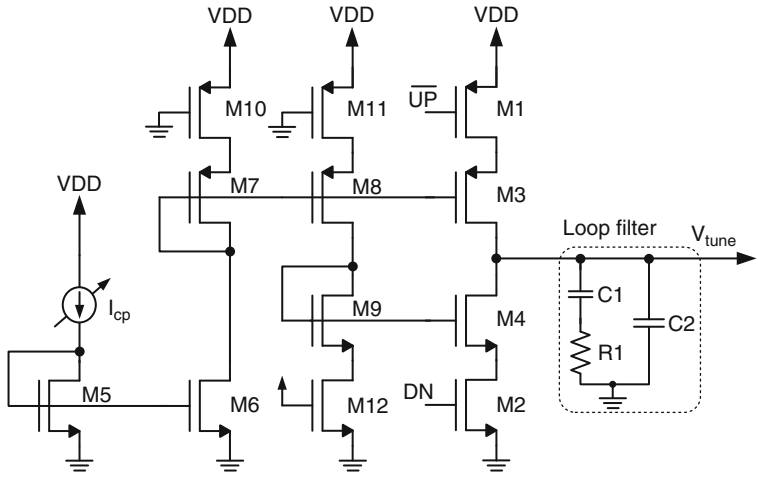

Fig. 5.13 Charge-pump schematic

the control voltage V_{tune} which, when up-converted by the VCO, manifests itself as discrete spurs in the output spectrum. This phenomenon, called reference feed-through can be characterized by determining the difference between the amplitude of the carrier and the reference spur. A large difference between these two implies a good matching between charge-pump current sources. The charge-pump implementation of this work is shown in Fig. 5.13. It consists of UP and DN switches M1 and M2, current source transistors M3 and M4, a variable current reference providing current I_{cp}, and current mirrors M5–M9. The dummy transistors M10–M12 are used to match the voltage drop across the switches, so that the current reference can be accurately mirrored to M3 and M4. The current mirror transistors are chosen to be three times the minimum channel length to achieve better matching between the UP

and DN currents (this approach increases the output impedance of the charge-pump thereby reducing the channel length modulation, which is a source of mismatch in current mirrors).The charge-pump current, according to Table 2.4, is chosen to be 500 μA and is adjustable by using a control voltage in the current reference circuit. Detailed simulations are carried out to match the two currents and to remove (or minimize) current spikes from the output pulses.

The last component of the synthesizer back-end is the loop filter which is also shown in Fig. 5.12. The job of the loop filter is to turn the charge-pump current into a stable DC voltage which could be utilized to control the VCO. In addition, it suppresses the high frequency components added by the pulsed operation of PFD and charge-pump. Furthermore, loop filters are also the components which control the overall loop dynamics and stability. The values of the second-order passive loop filter chosen for this work were calculated in Section 2.4.3. The three components of Fig. 5.12, including the loop filter, were simulated together to con-firm the correct control voltages of the charge pump (UP, DN). The considerations of integration of the loop-filter will be covered in Chapter 6.

5.3 Conclusions

This chapter presented the synthesizer back-end components which, although working at lower frequencies, entail challenges such as accuracy, matching and robustness. Two approaches have been presented for frequency division after the prescaler. First, is the cascade of divide-by-2 stages and second is the down-conversion utilizing a mixer. The former has been optimized for low power consumption by reducing the transistor dimensions and moderately increasing the load resistors. The mixer-based approach offers further reduction of power consumption. However, it requires a fixed and accurate LO for down-converting the prescaler output to a frequency close to the reference frequency of the synthesizer. Both these methods will be investigated during the complete synthesizer integration presented in the next chapter.

The design of the remaining back-end components namely phase-frequency detector, charge-pump and loop filter is also presented. The PFD is based on D-flip-flops constructed by custom made NAND gates. The dead-zone of the PFD is eliminated by inserting intentional delay in the reset path. The charge-pump is optimized for matching between up and down currents by using longer channel- and dummy transistors, for increasing the output impedance and identical voltage drop across transistors, respectively. The second order loop filter, combined with the PFD and charge-pump is simulated to confirm the correct loop polarity of the synthesizer.

Chapter 6
Synthesizer Integration

Abstract This chapter elaborates the integration of the complete synthesizer using the front-end and back-end components presented in the preceding chapters. In addition to the implementation and measurements of the 40 GHz synthesizer, the results of two other designs; first based on a mixer in the feedback loop and the second based on a complete dual-mode architecture for 40- and 60 GHz is presented.

Keywords Phase-locked loop · Frequency synthesizer · Phase noise · Settling time

The preceding chapters have presented the design of the synthesizer front-end and back-end components. The integration and measurements of the front-end components have also been presented which provide valuable experience and insight. Moving a step closer to the proposed synthesizer, this chapter covers the design and implementation of the complete synthesizer. The main challenge in the integration of high-frequency synthesizers is to synchronize the operating ranges of the VCO and the frequency dividers in the feedback loop. At such frequencies, interfacing of blocks with perfect frequency alignment is much more challenging than integrating blocks individually. This is because unexpected parasitics may cause significant frequency shift in the VCO or ILFDs, prohibiting the loop from locking. Therefore, careful co-design and simulations are required to characterize the performance of the complete synthesizer.

Section 6.1 presents the synthesizer implementation and measurement for the sliding-IF architecture for 60 GHz frequency down conversion. The issues encountered while interfacing the synthesizer components both at circuit and layout levels are discussed. Section 6.2 presents the synthesizer with a mixer in the feedback loop in place of a cascaded divider chain. This setup, completed up to layout, is based on a complete transistor level design including RC extraction of critical blocks. The proposed dual-mode synthesizer is discussed in Section 6.3 and utilizes the transistor level design of corresponding components from Chapter 4. Due to time and silicon-area limitations, the last design was not fabricated; however, its transistor level simulations utilize the measurement information obtained from individual component implementation.

H.M. Cheema et al., *60-GHz CMOS Phase-Locked Loops*,
DOI 10.1007/978-90-481-9280-9_6,

6.1 Synthesizer for 60 GHz Sliding-IF Frequency Conversion

The frequency conversion techniques for 60 GHz transceivers were categorized in Section 2.2. The sliding-IF technique (Fig. 2.5) down converts the RF signal in two steps by using 40 GHz ($f_{RF\text{-}LO}$ from the VCO) for the first down-conversion and 20 GHz ($f_{IF\text{-}LO}$ from the ILFD) for the second one. This section presents the design and implementation of a synthesizer suitable for the above mentioned architecture.

The complete synthesizer is shown in Fig. 6.1. As mentioned previously, the synchronized operation of different blocks is critical for correct overall performance. To this end, the individual component and front-end implementation in preceding chapters provides the starting point for the complete synthesizer integration. The front-end comprising of the VCO, quadrature ILFD and output buffers is almost identical to the one presented in Section 4.3.1. The measured locking range of the front-end was 37.6–42.2 GHz as opposed to the required range of 38–42.3 GHz. Therefore, the inductance of the VCO tank inductor is slightly tweaked to achieve the desired range. The ILFD presented in Section 4.1.3 demonstrates a locking range of 30–44 GHz which easily covers the required frequency range. However, its tank inductance is also lowered slightly to increase the center frequency. This assists in initiating lock with lower input power from the VCO. The tuning voltage from the loop-filter (V_{tune}) is utilized to simultaneously tune the VCO and the ILFD. Due to the limitation of on-wafer measurements, only the buffered output of the ILFD is transported to the bond-pads. The next component in the feedback loop is a selector block, which either passes the output of the ILFD or an external 20 GHz input (f_{ext}) to the divider chain. The latter is added to verify the functionality of the back-end in case the front-end frequency is off-target or suffers any other malfunction.

The divide-by-64 block consists of six cascaded divide-by-2 stages similar to the circuit presented in Section 5.1.1. Each divide-by-2 stage is based on CML D-latches, so the differential small-swing output from the last stage needs to be converted to rail-to-rail square pulses so that they could be compared to the reference pulses in the phase-frequency detector. This is achieved by a differential to single-ended converter followed by a pair of inverters as shown in Fig. 6.2. This setup consumes 0.2 mA from a 1.2 V supply. The rail-to-rail output is provided to the PFD and to a series of buffers for measurement purposes. This enables the observation of the divided frequency (f_{div}) and reference frequency (f_{ref}) in time-domain. The phase frequency detector and charge-pump designs are identical to the ones presented in Section 5.2. The reference frequency is provided by an external signal source and the two signal paths in the PFD and CP (for f_{ref} and f_{div}) are laid-out in a way to ensure symmetry and matching between them. The charge-pump current can be tuned externally by modifying a voltage in the current reference circuit. The second-order integrated loop filter consists of a resistor and two MIM capacitors. The relatively large 74.2 pF capacitor is formed by placing four smaller capacitors in parallel to achieve the required capacitance. Each sub-capacitor

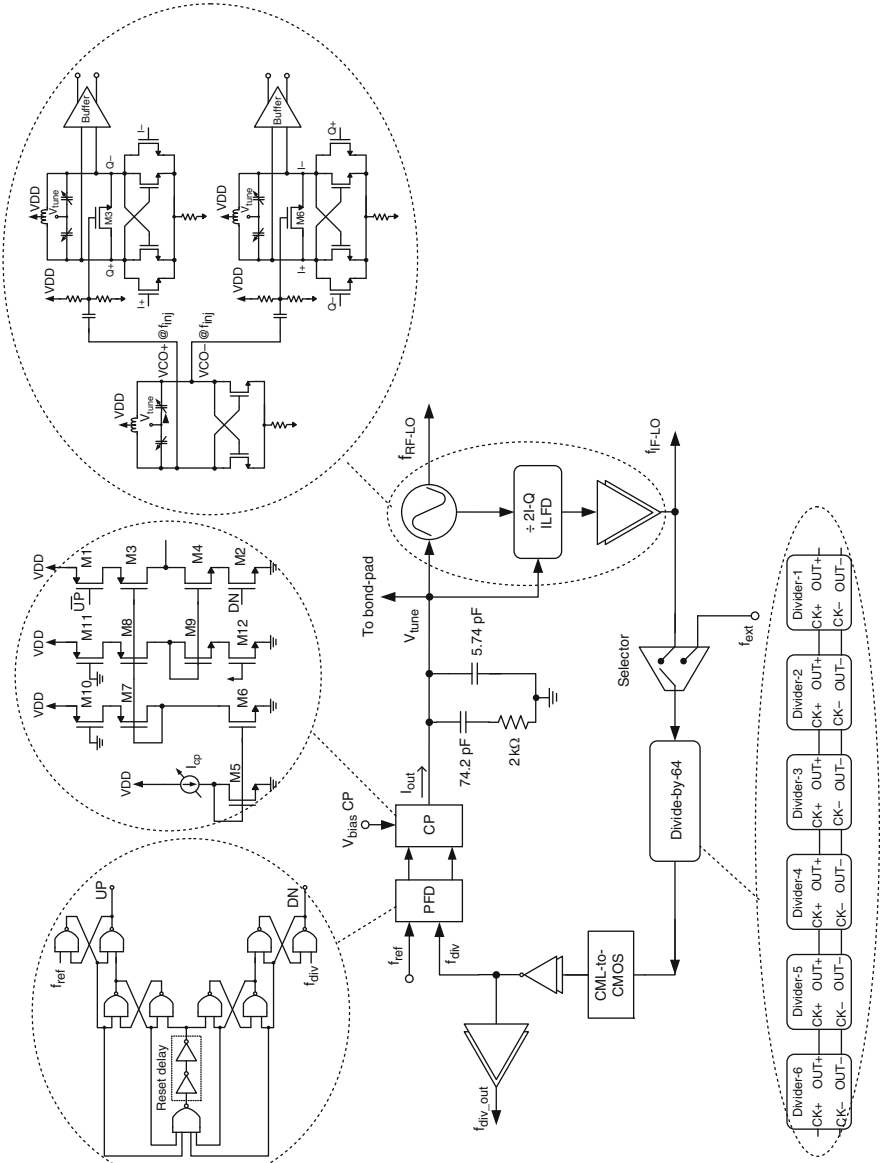

Fig. 6.1 Forty gigahertz synthesizer for 60 GHz sliding-IF down-conversion, underlying transistor level circuits shown in *dotted circles*

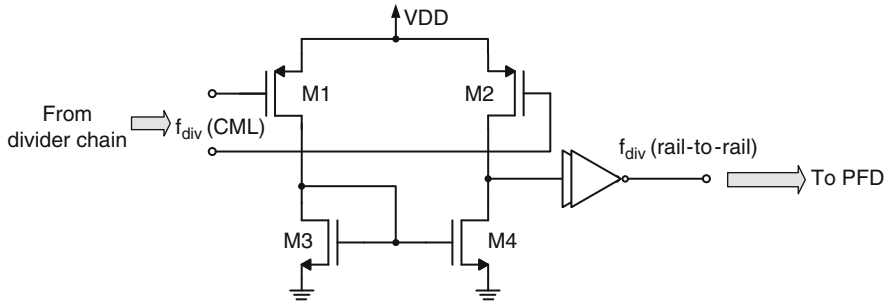

Fig. 6.2 CML to CMOS converter

contains multiple arrays of MIM structures which is a feature offered in the process design kit (PDK).

The overall circuit is simulated in Cadence™ to observe its locking and settling behavior. Transistor level simulation of a complete synthesizer is a painstaking task. Due to the largely different time constants of the front-end and back-end, a few micro-second transient simulation takes roughly 12–18 h to complete. Furthermore, memory requirements rise drastically if multiple node voltages and currents are to be saved. Running multiple simulations to verify correct operation for different reference frequencies further increases the design time. Therefore it is important to first verify the operation of individual components and then to combine them in steps. For instance, the front-end can first be combined with the divide-by-64 block to verify the correct output frequencies before connecting to the PFD. Similarly, the PFD, charge-pump and loop filter are simulated together to observe the output for varying input frequencies and phase differences. This approach somewhat reduces the number of simulations (hence the design time) required for the complete synthesizer. Transient simulation results for two different reference frequencies are shown in Fig. 6.3 where synthesizer locks to 39.6 and 41.5 GHz at the VCO output (or 19.8 and 20.75 GHz at ILFD output respectively).

The layout of the synthesizer is carried out following the best practices presented in Chapter 3. The resulting chip micrograph is shown in Fig. 6.4. The front-end layout, after modification in tank inductors of VCO and ILFD, is re-used from the previous iteration. Short RF interconnects, symmetry and isolation are features of the front-end layout. The divide-by-64 block follows the ILFD and as each divide-by-2 stage is optimized separately, the layout slightly varies for each stage. The PFD and charge-pump lie between the loop filter and the divide-by-64 block. It is evident that the integrated loop filter occupies the majority of the chip area. Transmission lines are used for all RF inputs and outputs including the reference frequency (f_{ref}) and divided output frequency (f_{div_out}). Although the TLs are not necessary for the latter, their construction including all metal layers assists in satisfying metal density requirements. De-coupling capacitors are placed for all supply voltages of the circuit. All the vacant chip-area is covered by arrays of

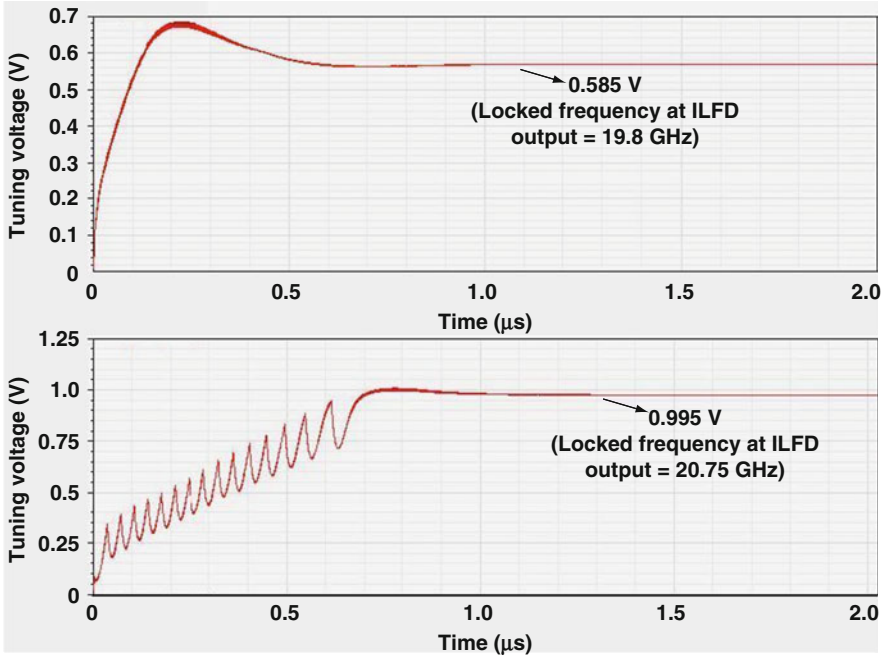

Fig. 6.3 Complete synthesizer transient simulation to verify settling time for $f_{ref} = 309.3$ MHz (*top*), and $f_{ref} = 324.2$ MHz (*bottom*)

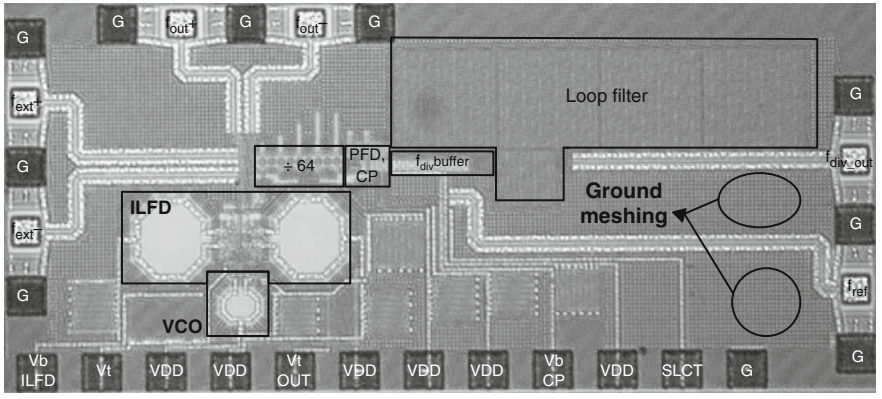

Fig. 6.4 Chip micrograph of the 40 GHz synthesizer

ground-meshing blocks similar to the one presented in Section 3.1.4. The total chip-are of the synthesizer including bond-pads is 1.67×0.745 mm^2.

In order to facilitate on-wafer measurements and avoid wire-bonding (or packaging), the DC inputs are provided to the circuit by using a 12-pin Eye-Pass probe

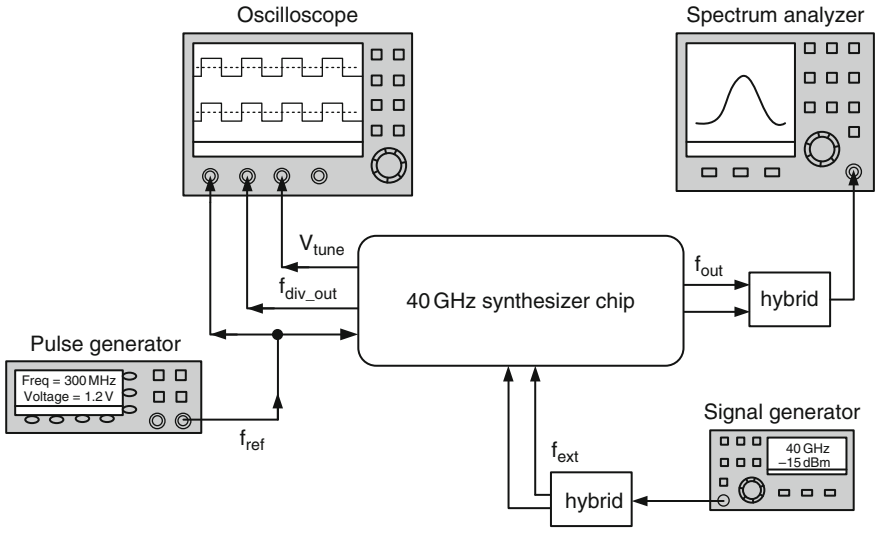

Fig. 6.5 Setup for 40 GHz synthesizer measurements

(from Cascade Microtech). The differential output (f_{out+} and f_{out-}) is obtained by a GSGSG probe and converted to single-ended by an external hybrid (from Krytar). The low frequency signals (f_{ref} and f_{div_out}) utilize the two signal pads separately. The measurement setup for the synthesizer is shown in Fig. 6.5.

The square-wave reference signal is provided by a pulse generator (Agilent 81134A) and also observed on the oscilloscope (LeCroy Wave Master 830Zi). The divided output frequency (f_{div_out}) and V_{tune} of the VCO are also observed on the oscilloscope. The differential output of the ILFD is provided to an Agilent spectrum analyzer (E4446A) with phase noise functionality. The "stand-by" input f_{ext} is supplied, if needed, to the synthesizer by an Agilent signal generator (E8257D).

The VCO, ILFD, and corresponding output buffer is first switched ON to observe the free-running center frequency of the front-end. The oscillation signal becomes visible at 1 V and for a nominal supply voltage of 1.2 V the VCO and ILFD consume 5 and 9 mA, respectively. The center frequency of the front-end is seen at 20.2 GHz. The divide-by-64 block is then included in the circuit by keeping the selector voltage HIGH and observing the divided frequency on the oscilloscope which in this case is ~315 MHz. The divide-by-64 circuit consumes 6 mW and the corresponding output buffer which is a cascade of four inverter stages consumes 2 mW. The reference frequency equal to the divided frequency is then injected to the circuit and also observed on the oscilloscope.

The reference signal is varied in steps from 290 to 344 MHz, which corresponds to an output frequency of 18.5–22 GHz (or 37–44 GHz at the VCO output). From these values, the ILFD output of the synthesizer locks between 19.1 and 21.8 GHz. The corresponding locked frequency range at the VCO output is 38.2–43.6 GHz.

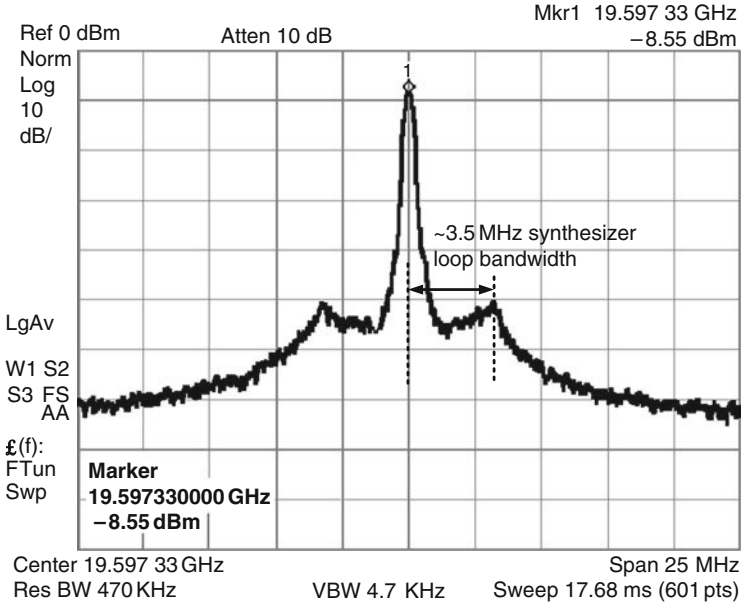

Fig. 6.6 Locked synthesizer spectrum for $f_{ref} = 306.2$ MHz

The synthesizer can thus down-covert a 60 GHz signal within a range of 57.3–65.4 GHz (three times the ILFD output or 1.5 times the VCO output frequencies). A locked spectrum screenshot for a reference frequency of 306.2 MHz is shown in Fig. 6.6. In a typical synthesizer, the sideband spectrum noise is cleaned-up within the loop bandwidth which is evident by the highlighted area in Fig. 6.6. The loop bandwidth estimated from the spectrum screenshot is about 3.5 MHz as opposed to the calculated value of 4 MHz (in Section 2.4.3). The output power of −8.55 dBm also includes the 1.5–3 dB of cable and other measurement related loss.

In order to view the settling behavior of the synthesizer, we recall from Table 2.2c that for the first two 2 GHz HRP channels at 57.6 and 59.4 GHz, the corresponding frequencies at the ILFD output are 19.2 and 19.8 GHz. This translates to a reference frequency step of about 9.4 MHz. Setting the synthesizer output at its lowest end with a reference frequency of 299.2 MHz, a step of 9.4 MHz is given to change it to 308.6 MHz. As the settling time is in micro-second range the change in tuning voltage is not visible by naked eyes. Therefore, the data is saved to memory in the oscilloscope and plotted in Fig. 6.7. The measured settling between adjacent HRP channels is about 1.1 μs. Similarly, the settling behavior for a "jump" between the first and last HRP channel is observed and the maximum settling time observed is ∼2 μs with some cycle-slipping also visible.

An oscilloscope screenshot of the time-domain representations of the reference frequency and the divided frequency after locking is shown in Fig. 6.8. The cause of distortion in the f_{ref} signal is not completely clear. It is thought of to be due to the settings of the oscilloscope or a measurement error.

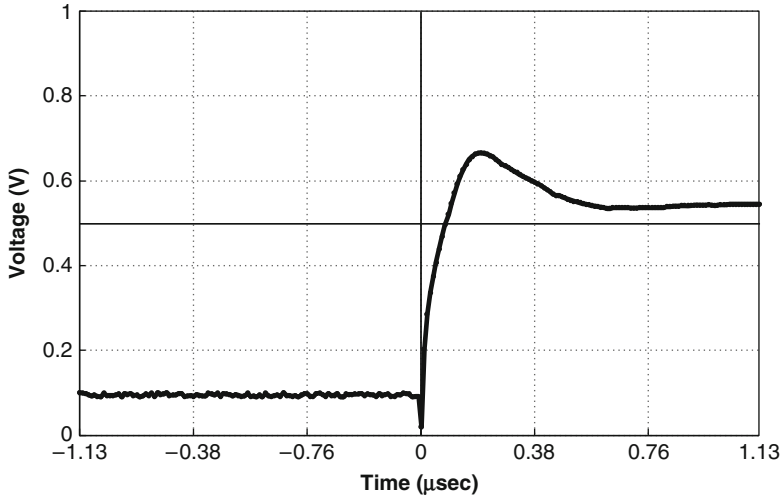

Fig. 6.7 Measured settling behavior for a 9.4 MHz reference frequency step, corresponding to shifting from 57.6 and 59.4 HRP channels

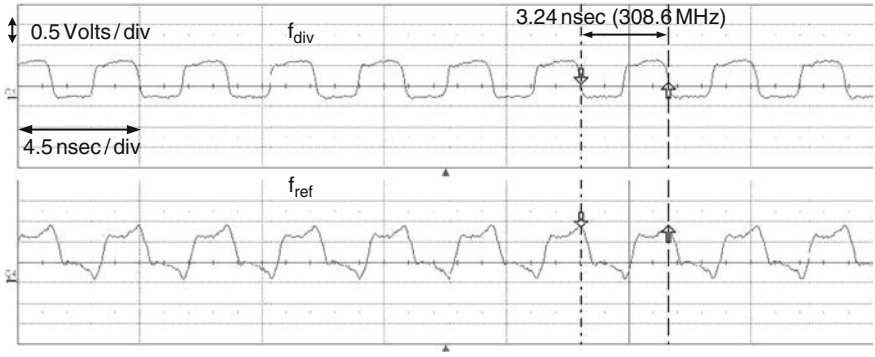

Fig. 6.8 Measured time-domain signals f_{div} and f_{ref} after locking to a 9.4 MHz step

The phase noise of the synthesizer is measured by the spectrum analyzer at the ILFD output and reflects its loop performance. Figure 6.9 shows the phase noise plot for a locked frequency of 20.12 GHz from 100 kHz to 100 MHz. The value at 1, 4 and 10 MHz offset from the carrier is −95.7, −100 and −118 dBc/Hz, respectively. The first of the above values is the in-band phase noise (within the loop bandwidth), the second at the calculated loop bandwidth (forming the "knee" in the overall plot) and the third corresponds to the out-of-band phase noise value. The variation of phase noise over the synthesizer operation range is ±2.5 dB. The phase noise at the VCO output (at double the frequency) can be estimated by adding 6 dB to the above mentioned values, resulting in −89.7, −94 and −112 dBc/Hz at 1, 4

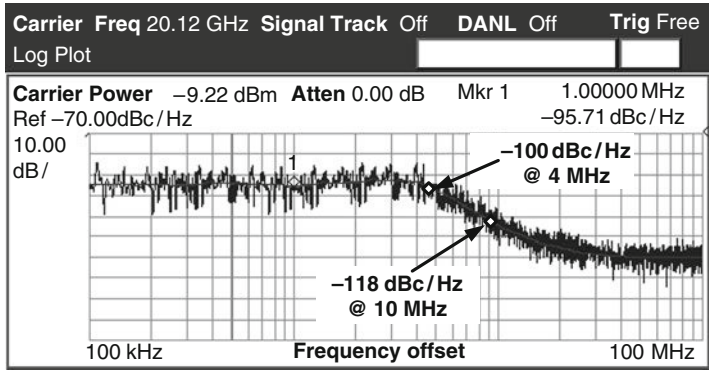

Fig. 6.9 Phase noise of the synthesizer at 20.12 GHz (measured at ILFD output)

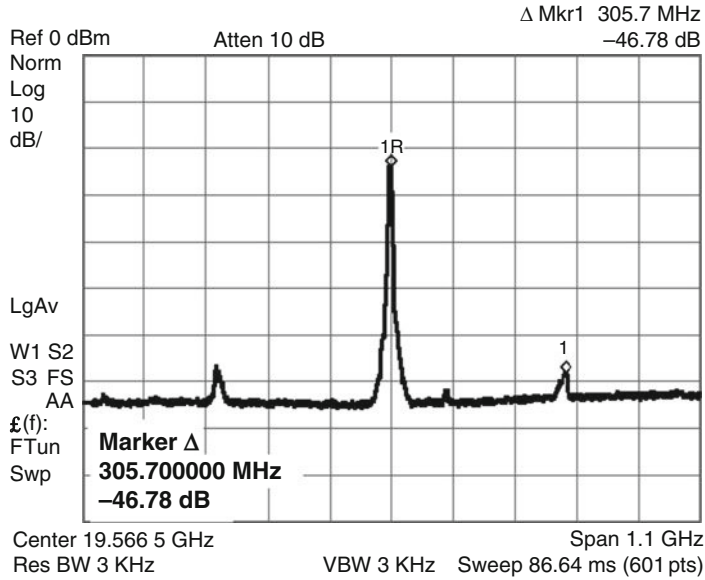

Fig. 6.10 Output spectrum with 1.1 GHz span to show reference spurs at 305.7 MHz for a synthesized frequency of 39.12 GHz

and 10 MHz offset from the carrier. In Section 2.5 it was explained that, outside its loop bandwidth, the synthesizer phase noise is dominated by the VCO. This is confirmed by the measured value at 10 MHz offset (−118 dBc/Hz) which is within ±0.4 dB of the corresponding measured value of the 40 GHz synthesizer front-end in Section 4.3.1 (Fig. 4.82).

Due to the finite mismatches in the PFD and charge pump, reference spurs are observed at the output. One such example is depicted in Fig. 6.10. The reference

Table 6.1 Summary of 40 GHz synthesizer performance

Locked frequencies	19.1–21.8 GHz
	Corresponding to 38.2–43.6 at 40 GHz and 57.3–65.4 GHz at 60 GHz
Phase noise at ILFD output	−94 to −97 dBc/Hz @ 1 MHz offset −99.5 to −101 dBc/Hz @ 4 MHz offset −117 to −119.5 dBc/Hz @ 10 MHz offset
Estimated phase noise at VCO output	−88 to −91 dBc/Hz @ 1 MHz offset −93.5 to −95 dBc/Hz @ 4 MHz offset −111 to −113.5 dBc/Hz @ 10 MHz offset
Settling time	<2 μs
Reference spurs	<−42 dBc
Output power at ILFD Output	−5 to −8.5 dBm
Supply voltage	1.2 V
Power consumption	
VCO	6 mW
I-Q ILFD	9 mW
Divide-by-64	6 mW
PFD and CP	1.8 mW
Buffers	14 mW
Total (excluding buffers)	22.8 mW
Total (including buffers)	36.8 mW
Chip area	1.67×0.745 mm^2
Technology	65 nm CMOS

spurs are 46 dB below the carrier at 19.56 GHz. At higher frequencies the reference spurs are stronger due to increased VCO gain; the worse-case spurs are 42 dB below the carrier power. The output power of the synthesizer after de-embedding the measurement losses is between −5 and −8.5 dBm. The synthesizer consumes 22.8 mW from a 1.2 V supply in total without buffers, and 36.8 mW with buffers. The summary of the synthesizer performance is presented in Table 6.1.

6.1.1 Comparison to Target Specifications

The measured results of the 40 GHz synthesizer fulfill the target specifications laid-out in Section 2.6 quite closely. The operation range of 38.1–43.6 GHz is wider than the required 38–42.3 GHz. The average in-band phase noise at 40 GHz is 5.5 dB worse than the target whereas out-of-band phase noise is 2 dB better than the target value of −110 dBc/Hz. The measured settling time for stepping between adjacent channels is 1.1 μs which is close to the target of ∼1 μs. However, for larger frequency steps it increases to ∼2 μs. Although no specifications were required for reference spurs, the measured level of −42 dBc below the carrier is comparable to published works [69, 139]. The output power levels at the ILFD output are high enough to drive subsequent circuits and the total power consumption of 22.8 mW is also quite low for a 40 GHz synthesizer.

6.2 Synthesizer with Down-Conversion Mixer in Feedback Loop

The replacement of the divider chain in the feedback loop with a mixer was proposed in Section 5.1.2. This approach simplifies the division and also reduces the power consumption of the synthesizer. In this section, a single-balanced mixer analyzed in the Section 5.1.2 is included in the synthesizer loop and simulated for performance comparison with the synthesizer with feedback divider. The complete synthesizer is shown in Fig. 6.11 with highlighted mixer in the feedback loop. The transistor level circuits of the remaining components are identical to Fig. 6.1. The reference frequency ($f_{ref\text{-}mixer}$) is provided to the mixer by a signal source and is

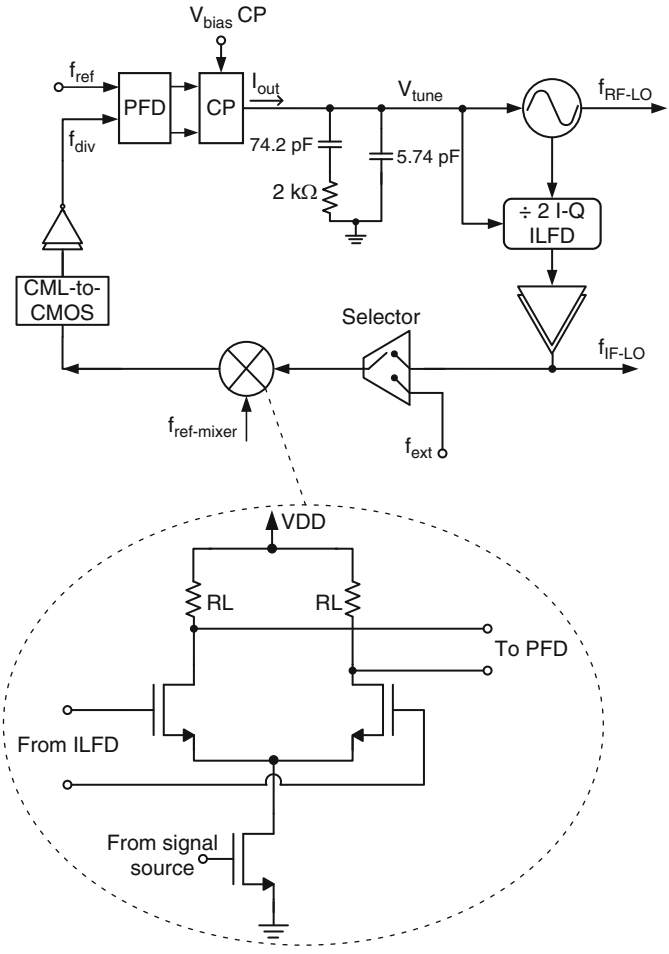

Fig. 6.11 Forty gigahertz synthesizer with mixer in feedback loop

assigned in such a way that the down-converted frequency f_{div} in steady state is always 300 MHz. The output frequency of the synthesizer is stepped-up (or down) by varying the mixer reference frequency ($f_{ref\text{-}mixer}$) and can be expressed as

$$f_{RF-LO} = 2\left(f_{ref} + f_{ref-mixer}\right) \quad \text{and} \quad f_{IF-LO} = f_{ref} + f_{ref-mixer} \tag{6.1}$$

Fixing the reference frequency to 300 MHz, the required range of $f_{ref\text{-}mixer}$ to obtain the target frequency range is 18.7–21 GHz. Adopting these settings, the synthesizer's working range easily satisfies the desired frequency range of 38–42.3 GHz. The settling behavior of the synthesizer is different than for the feedback divider case, as the injection locking in the front-end is instantly followed by the down-conversion by the mixer. This is different than the divider chain in which the signal sequentially passes through a number of stages before comparison in the PFD. Due to above mentioned reasons, the initial changes in the tuning voltage are quite profound but the loop reacts very fast resulting in a short settling time. Two examples of the simulated transient response are shown in Fig. 6.12 where the output frequencies $f_{RF\text{-}LO}$ of 41.5 and 38.8 GHz are generated and the settled tuning voltage is 0.856 and 0.488 V, respectively. The settling time is ~0.7 μs which is almost half as compared to the synthesizer with feed- back divider. The initial tuning voltage is clamped to 1.2 V; however, similar results are obtained otherwise (for zero initial voltage). The power consumption of the synthesizer is reduced to 17.4 mW without buffers as compared to 22.8 mW of the measured synthesizer of Section 6.1. This improvement is due to the replacement of the divide-by-64 block which consumes 6 mW with a mixer only dissipating 0.6 mW. The layout of the

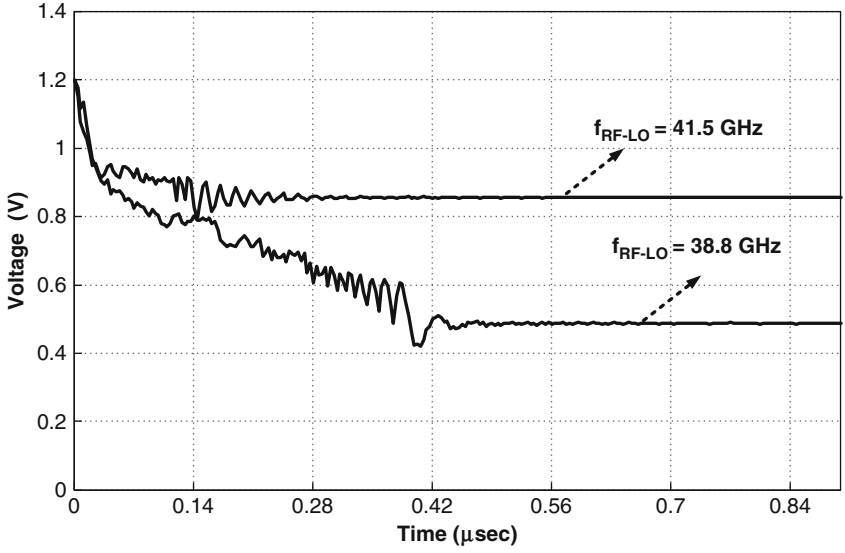

Fig. 6.12 Simulated settling behavior of a 40 GHz synthesizer with mixer in the feedback loop

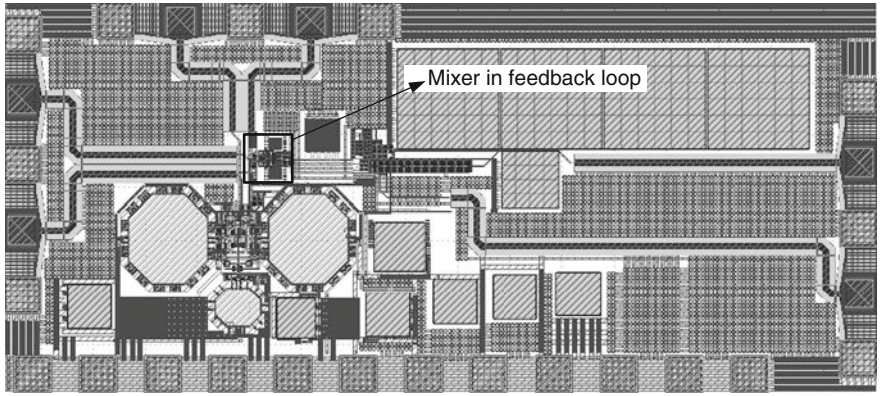

Fig. 6.13 Layout of 40 GHz synthesizer with mixer in feedback loop

Table 6.2 Mixer based 40 GHz synthesizer performance summary

Output frequency ($f_{RF\text{-}LO}$)	38–42.5 GHz
Settling time	$<$1.2 µs
Supply voltage	1.2 V
Power consumption	
VCO	6 mW
I-Q ILFD	9 mW
Mixer	0.6 mW
PFD and CP	1.8 mW
Buffers	14 mW
Total (excluding buffers)	17.4 mW
Total (including buffers)	31.4 mW

mixer-based synthesizer (to be taped-out) is shown in Fig. 6.13 where the divide-by-64 block is replaced by the mixer occupying a much smaller area than the former component. The simulated performance of the mixer based 40 GHz synthesizer is summarized in Table 6.2.

6.3 Dual-Mode Synthesizer

The preceding sections presented the single-mode 40 GHz synthesizer using a cascaded divider-chain or a mixer in the feedback loop. Combining the two synthesizer front-ends of Chapter 4, this section presents the proposed dual-mode synthesizer (of Section 2.3). The complete synthesizer along with the underlying circuit schematics of the VCOs and dual-mode ILFD is shown in Fig. 6.14. The back-end remains unchanged and the transistor level implementation of the other components is identical to the design in Fig. 6.1. The two VCOs can be included or excluded from the loop for instance by switching their respective supply voltage ON or OFF. The outputs of both VCOs are provided to the dual-mode ILFD which,

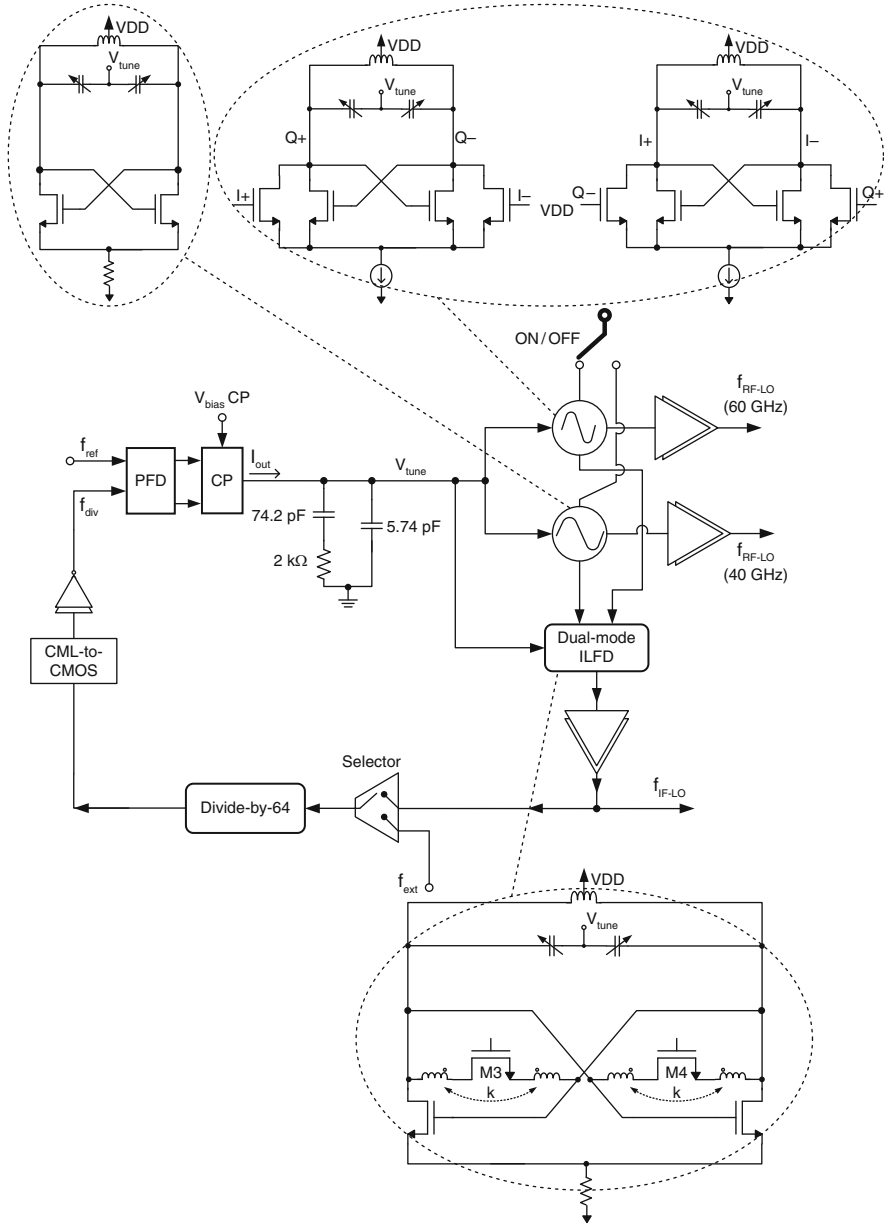

Fig. 6.14 Dual-mode synthesizer for sliding-IF and direct conversion transceiver with underlying transistor level circuit schematics of the high frequency components. The remaining components have the same transistor level implementation as Fig. 6.1

along with the VCOs is tuned by the loop filter's output. For a direct-conversion receiver, the 60 GHz VCO output provides the $f_{RF\text{-}LO}$ and is applied to the output buffers. On the other hand, for the sliding-IF case, outputs of the 40 GHz VCO and ILFD are buffered and provide the $f_{RF\text{-}LO}$ and $f_{IF\text{-}LO}$, respectively.

In order to verify the locking range and transient behavior of the dual-mode synthesizer, the transistor level circuit is simulated in Cadence™. For a fixed division ratio of 128, the reference frequency needs to be modified in two separate ranges. If the 40 GHz VCO is switched ON, it has to be varied between 290 and 340 MHz whereas if the 60 GHz VCO is ON the reference frequency range is 445–500 MHz. First, the 60 GHz VCO is enabled to synthesize the corresponding frequencies. Based on the measured results of the VCO and the dual-mode ILFD, their tuning and locking ranges are synchronized by tweaking the tank values. Recalling from Table 2.3, the output frequency range required at 60 GHz spans from 57 to 63.6 GHz. To step from one LRP channel of 500 MHz, the reference frequency has to be stepped by 4.68 MHz. Similarly, for HRP channels of 1 and 2 GHz, the required reference frequency increment or decrement is 14.06 MHz.

Each core of the 60 GHz I-Q VCO is biased at 10 mA and consumes 24 mW in total from a 1.2 V supply whereas the dual-mode ILFD consumes 4 mW from a 0.8 V supply. The synthesizer is able to generate frequencies between 57 and 63.5 GHz which covers 11 out of 12 LRP channels and all four HRP channels. The last LRP channel (C12 in Table 2.3) having a center frequency of 63.6 GHz cannot be generated with the limited voltage supply of 1.2 V. However, if the supply voltage in the CML-to-CMOS converter block, PFD and charge-pump is increased to 1.4 V, the FTR of the VCO is extended to 63.9 GHz and the synthesizer can lock to the C12 channel at 63.6 GHz. The settling behavior of the synthesizer for a reference frequency of 487.5 MHz is depicted in Fig. 6.15. The simulated settling time of the synthesizer is less than 1.8 μs.

On the other hand, enabling the 40 GHz VCO reproduces the results presented in Section 6.1 and the synthesizer is able to provide locked frequencies between 38 and 43.5 GHz at the VCO output and 19 and 21.75 GHz at the dual-mode ILFD output. The 40 GHz VCO consumes 6 mW from a 1.2 V supply. The total front-end power consumption including both the VCOs and dual-mode ILFD is 34 mW. The back-end consumes 7.8 mW and the three output buffers consume 30 mW in total from a 1.2 V supply.

The simulated results of the dual-mode synthesizer are summarized in Table 6.3 and closely satisfy the target specifications laid out in Section 2.6. The locking range for the sliding-IF is larger than the required 38–42.3 GHz whereas for a loop filter voltage range of 0–1.2V, the direct-conversion falls 100 MHz short of the desired locking range. The maximum settling time for both modes of operation is 1.8 μs. The power consumption of 42 mW for the dual-mode synthesizer excluding buffers is either comparable or lower than published single-mode synthesizers, for instance [24, 139]. The phase noise of the dual-mode synthesizer can be split into two parts, the in-band phase noise which mainly depends on the synthesizer back-end can be estimated by the measured results of the 40 GHz synthesizer in Section 6.1 and lies between −88 and −91 dBc/Hz (Table 6.1). The out-of-band

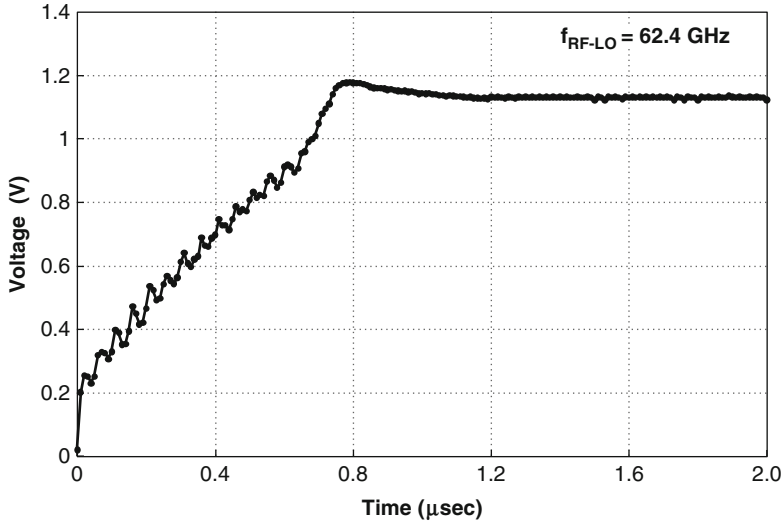

Fig. 6.15 Settling of the dual-mode synthesizer for a 60 GHz synthesized frequency

Table 6.3 Summary of the dual-mode synthesizer performance

Output frequency ($f_{RF\text{-}LO}$) for direct-conversion	57–63.5 GHz
Output frequencies ($f_{RF\text{-}LO}$ and $f_{IF\text{-}LO}$) for sliding-IF	38–43.5 and 19–21.75 GHz
Settling time	$<$1.8 μs
Supply voltage	1.2 and 0.8 V
Power consumption	
40 GHz VCO	6 mW
60 GHz I-Q VCO	24 mW
Dual-mode ILFD	4 mW (0.8 V supply)
Divide-by-64	6 mW
PFD and CP	1.8 mW
Buffers	32 mW
Total (excluding buffers)	41.8 mW
Total (including buffers)	73.8 mW

phase noise follows the VCO, so two separate values are obtained. For the 40 GHz synthesizer it lies between −111 and −113.5 dBc/Hz at 10 MHz offset, whereas for the 60 GHz synthesizer it can be estimated by the measured VCO phase noise (Section 4.2.4; Fig. 4.64) and is better than −115 dBc/Hz.

6.4 Conclusions

In this chapter, building on the components and sub-circuit designs of preceding chapters, complete synthesizers based on our proposed flexible architecture are presented. The 40 GHz VCO, ILFD and synthesizer front-end integration in

Chapter 4 provide vital experience related to shift between simulations and measurements. Using this expertise, the integration of the complete synthesizer is considerably simplified and the measured and simulated results match very closely. Based on the 40 GHz components, a single-mode synthesizer for 60 GHz sliding-IF system is presented first. It demonstrates sufficient locking range to cover the 60 GHz frequency band from 57 to 65 GHz. The next synthesizer replaces the divider chain in the feedback loop with a mixer operated by an external LO signal. Fixing the reference frequency, the output of the synthesizer is stepped-up and down by varying the mixer LO frequency. This setup offers savings in silicon area and power consumption but has a drawback of an extra LO frequency.

Combining the two synthesizer front-ends and replacing the single-mode ILFD with the dual-mode ILFD, a dual-mode synthesizer is presented. In the 60 GHz mode, it is noticed that the tuning-range of the VCO is a limiting factor to cover the complete frequency range and the presented design can only cover 11 out of twelve 500 MHz LRP channels. On the other hand, in the 40 GHz mode, the synthesizer is able to cover the locking range requirement successfully. The synthesizer provides an elegant solution for sliding-IF as well as direct-conversion transceivers with or without using a frequency tripler. Although due to time and fabrication limitations, only the sliding-IF version was measured, based on the 60 GHz individual front-end components measured in preceding chapters, the simulation results of the dual-mode version can be considered fairly accurate. This version will be part of future research and implementation work.

Chapter 7
Conclusions

Abstract As a conclusion of the book, this chapter summarizes the challenges for 60 GHz integrated circuit design and their solutions presented in this book.

Keywords Systematic design · Multi-mode operation · 60 GHz

This book presents a systematic design and implementation of flexible frequency synthesizers for 60 GHz wireless transceivers. Based on the gained experience, it can be said that sub-nanometer bulk CMOS technologies have the market potential for 60 GHz systems. It has been demonstrated that dividing the system into sub-blocks and further down into components, and their implementation in the reverse order, is the right way to go, as the direct integration of complete system entails a high risk of failure.

We have demonstrated the design, implementation and verification of all the critical components of the synthesizer such as VCOs, single-mode and dual-mode prescalers suitable for 40 and 60 GHz operation. Furthermore, these components are integrated step-wise, first as synthesizer front-ends and finally in a complete synthesizer along with the back-end components.

The impact of parasitics is found to be significant at 60 GHz. The extraction tools and EM simulators are still not accurate enough. This causes a drift in comparison with the target specifications. Therefore, a successful and accurate system design requires a number of iterations and based on the positive or negative shift in a specific iteration, the subsequent one must be updated accordingly. Furthermore, it is important to incorporate the parasitic effects at an early stage of circuit design to reduce the design time.

The layout is another critical design step for 60 GHz systems. For mm-wave layout there are no-rules but only guidelines. We have shown that distributed analysis at mm-wave frequencies is not only required due to small wavelengths but also because the interconnect parasitics become of the same order as the passive structures. Therefore, a minimum tolerable interconnect length based on the

H.M. Cheema et al., *60-GHz CMOS Phase-Locked Loops*,
DOI 10.1007/978-90-481-9280-9_7,

operation frequency and the circuit application needs to be determined. It is also shown that not only the individual layout of passives (such as inductors and transformers) is important, but also the overall layout environment around them, has a significant impact on their performance. Thus, characterization of the overall core layout using EM simulators is necessary for confirming the correct and expected circuit operation. However, it is also observed that EM simulation of such complete layouts is a tedious and complex task as it includes multiple I/O ports, interconnects and vias. Furthermore, for these overall simulations, we have demonstrated that it is essential to verify the correctness of the obtained results by simplified and/or indirect simulations.

The measurements of 60 GHz circuits and systems are extremely challenging and require specialized techniques and equipment. It is shown that contact probing, sensitivity to external noise, cable losses and other related non-idealities need to be carefully encountered to extract reliable measurement results at such high frequencies.

Appendix

Appendix A

A Travelling Wave Divider Simulation Results

The travelling wave divider was introduced in Section 4.1.1 as a prescaler choice for the proposed synthesizer. Transistor level simulations were carried out to observe its mm-wave performance. A sinusoidal signal with maximum amplitude of 300 mV is used as an input clock signal whereas I_{tail} used is 10 mA (See Fig. 4.6). Optimization of the circuit involves minimizing parasitic capacitance at the drain nodes of M1–M4 to speed-up the charging while keeping enough gain in the loop. An optimized value of 160 Ω is used as the load resistance.

The input sensitivity of the TWD is estimated by reducing the input amplitude for each input frequency such that the divider still operates correctly yielding a divide-by-2 output. Shown in Fig. A.1 (black curve), the divider can operate from 22 to 45 GHz with a minimum and maximum input power of −26 and 2 dBm, respectively. The broadband operation of the TWD is seen by calculating the locking range (LR) using (4.3) and is equal to 68%. There are two down-sides of the TWD revealed by simulations. Firstly, the maximum and minimum operation frequency is susceptible to load resistance variation. For a ±10% variation (nominal for CMOS technologies) the locking range of the divider is affected as shown in Table A.1.

It is therefore necessary to cater for this variation and slightly overdesign to meet the required locking range. The other, more important, disadvantage of the TWD is the considerable variation of output amplitude over the locking range. This occurs due to reduction of gain of transistors M1–M5 as the clock frequency increases. This variation can de-sensitize the following divider stages which might require higher input amplitude for proper division. Thus, the design of TWD should be carried out together with the components it needs to drive in the overall system. The variation of amplitude is shown in Fig. A.1 (grey curve).

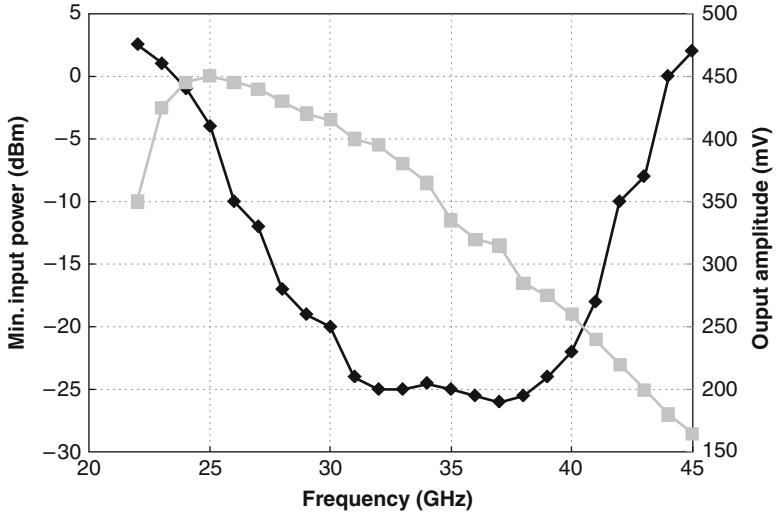

Fig. A.1 Input sensitivity (*black*) and output amplitude variation (*grey*) of a travelling wave divider

Table A.1 Variation of locking range of TWD with load resistance

Load resistance (R_L)	Locking range (GHz)
160 Ω	22–45
144 Ω (−10%)	24–45
176 Ω (+10%)	22–43

Appendix B

B LC-VCOs Theory

Oscillators in general can be analyzed by modeling them as feedback systems. Figure B.1 shows a general block diagram of a feedback system with transfer functions G(jω) and H(jω). The transfer function of this system can be given as

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{G(j\omega)}{1 - G(j\omega)H(j\omega)} = \frac{G(j\omega)}{1 - T(j\omega)} \tag{B.1}$$

where T(jω) = G(jω) H(jω) is called the loop gain. If the loop gain goes to one at a certain frequency ω_0, the transfer function goes to infinity. Thus the system becomes unstable and begins to oscillate at ω_0 in response to any "disturbance" in the system. The necessary conditions for oscillation can be summarized as

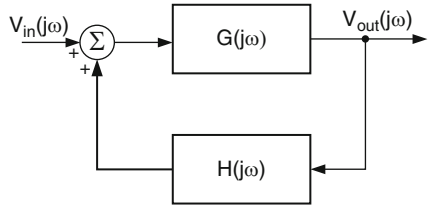

Fig. B.1 Oscillator feedback model

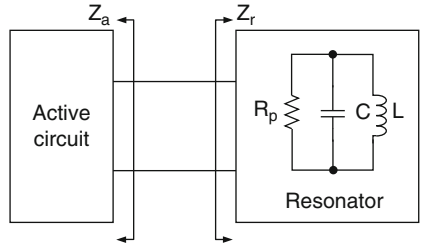

Fig. B.2 Oscillator negative resistance model

$$|G(j\omega)\,H(j\omega)| = 1 \angle |G(j\omega)\,H(j\omega)| = k \cdot 360^{\circ} \tag{B.2}$$

Termed as the Barkhausen's criteria, the gain and phase condition of (B.2) state the necessary requirements for stable oscillation, but not the start-up. In order to guarantee oscillator start-up, the loop gain must initially be larger than unity. In physical circuits, once this condition is satisfied, the circuit noise, an initial condition or a small current or voltage pulse can kick-start the oscillator. Ideally these oscillations are expected to grow indefinitely but as the oscillation amplitude increases, the non-linearity (and eventually saturation) limits the maximum amplitude. In other words, the poles in the right half plane during growing oscillations eventually move to the imaginary axis to stop the growth and the loop gain becomes unity for steady-state oscillations.

The second model utilized widely for oscillator (especially LC-VCOs) analysis is the so-called negative resistance model which can be regarded as a special case of oscillator feedback model. As shown in Fig. B.2, the oscillator can be divided into two parts, a resonator and an active circuit block. An ideal resonator can sustain its oscillation indefinitely. However, in practice some of the energy circulating in the tank is lost in its resistance R_p in every cycle, thus ceasing the oscillation with time. If an active circuit connected to the resonator, generates a resistance equal to $-R_p$, the loss of the tank can be compensated and a sustained oscillation can be achieved. In other words, the energy lost in R_p is replenished by the active circuit in every cycle. Mathematically, this can be expressed in terms of impedance of the blocks as

$$Z_a(j\omega) = R_a(j\omega) + jX_a(j\omega) \quad \text{and} \quad Z_r(j\omega) = R_r(j\omega) + jX_r(j\omega) \tag{B.3}$$

where the subscripts 'a' and 'r' refer to the active and resonator blocks. The oscillation conditions for the negative resistance model can be written as

$$\begin{aligned} R_a(j\omega) + R_r(j\omega) &= 0 \\ X_a(j\omega) + X_r(j\omega) &= 0 \end{aligned} \tag{B.4}$$

At the resonance frequency of the tank, the reactance of the inductor and capacitor cancel out, thus, the role of the active part is to cancel the real part in the impedance equation by generating a negative resistance equal to the equivalent resistance of the tank. As in the feedback model, the above conditions are for stable oscillation and in order to ensure oscillator start-up in actual circuits, the negative resistance is kept two to three times larger than the resonator resistance.

It is evident from the negative resistance model explained above that in order to ease oscillation start-up, the loss in the resonator should be as small as possible. This loss is quantified by the well-known quality factor (Q-factor) of the tank which is a measure of the energy stored and the power dissipated during each oscillation cycle, i.e.

$$Q = \omega \frac{E_{stored}}{P_{diss}} \tag{B.5}$$

Prior to determining the Q-factor of the tank, it is pertinent to summarize the corresponding Q-factor of the inductor and capacitor that make up the tank. To this end, it can be observed that loss of an inductor or capacitor can be represented either as a series or a parallel resistance. Shown in Fig. B.3a, the Q-factor of an inductor with series resistance can be calculated using (B.5) as

$$Q_{Ls} = \omega \frac{1/2 I^2 L}{1/2 I^2 R_{Ls}} = \omega \frac{L}{R_{Ls}} \tag{B.6}$$

If the impedance of the same setup is written as $Z_L = R_{Ls} + j\omega L$, it can be seen from (B.6), that the Q-factor of an inductor is the ratio of imaginary and real part of

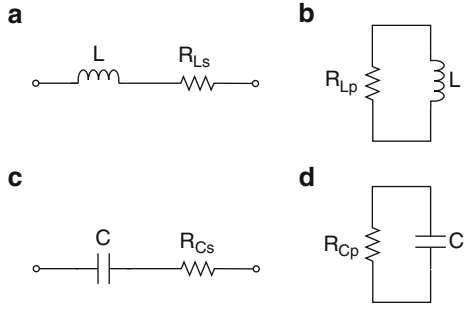

Fig. B.3 Inductance and capacitance with series and parallel resistances. Subscripts 'C' and 'L' stand for capacitance and inductance and 's' and 'p' refer to series and parallel connection

its impedance, which is another well-known definition of inductor quality factor. Similarly, the Q-factor of the parallel equivalent can be written as

$$Q_{Lp} = \omega \frac{1/2\, L\left[V^2 \Big/ (\omega L)^2\right]}{1/2\, \left[V^2/R_{Lp}\right]} = \frac{R_{Lp}}{\omega L} \tag{B.7}$$

If the two circuits are equivalent, then $Q_{Ls} = Q_{Lp} = Q_L$ and equating (B.6) and (B.7) yields

$$R_{Lp} = Q_L^2 R_{Ls} \tag{B.8}$$

The Q-factor for the capacitor with series and parallel resistance can also be computed similarly and is given below

$$Q_{Cs} = \frac{1}{\omega C R_{Cs}} \quad \text{and} \quad Q_{Cp} = \omega C R_{Cp} \tag{B.9}$$

The relation between series and parallel resistance for capacitors is given by

$$R_{Cp} = \frac{R_{Cp}}{Q_C^2} \tag{B.10}$$

The Q-factor of the LC-tank can now be calculated using the series or parallel setup of inductor and capacitor. Figure B.4 shows the latter combined in form of an LC-tank. It is evident that the parallel resistances of the capacitor and inductor can be lumped into one resistance R_p. Using (B.7) and (B.9), R_p can be written as

$$R_p = R_{Cp} \parallel R_{Lp} = \frac{\frac{Q_{Cp}}{\omega C} \cdot \omega L Q_{Lp}}{\frac{Q_{Cp}}{\omega C} + \omega L Q_{Lp}}$$

After some re-arranging, R_p can be written as

$$R_p = \sqrt{\frac{L}{C}}\left[\frac{Q_{Cp}\, Q_{Lp}}{Q_{Cp} + Q_{Lp}}\right] \tag{B.11}$$

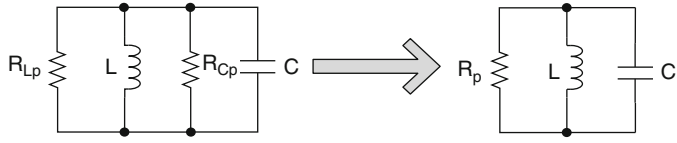

Fig. B.4 Combining parallel resistance of capacitor and inductor to determine tank Q-factor

It is interesting to determine the tank Q-factor in terms of Q_{Cp} and Q_{Lp}. To this end, it can be proven that for a standard RLC circuit, the resonance frequency ω_0 and corresponding Q-factor is given by

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad \text{and} \quad Q|_{\omega=\omega_0} = R\sqrt{\frac{L}{C}} \tag{B.12}$$

Using (B.12) in (B.11), the Q-factor of the tank can be given as

$$Q_{\text{tank}} = \frac{Q_{Cp}\, Q_{Lp}}{Q_{Cp} + Q_{Lp}} \tag{B.13}$$

As the series and parallel set-ups are equivalent, the subscripts 'p' can be omitted to obtain

$$Q_{\text{tank}} = \frac{Q_C\, Q_L}{Q_C + Q_L} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{B.14}$$

Equation (B.14) provides a few insights about the dependence of tank Q-factor on individual Q-factor of its components and is discussed further in Section 4.2.2. Furthermore, tuning range expressions including the impact of fixed and parasitic capacitance and phase noise characteristic is also discussed in the above mentioned section.

References

1. Su Khiong Yong, Chia-Chin Chong, An overview of multigigabit wireless through millimeter wave technology: potentials and technical challenges. EURASIP J. Wireless Commun. Networking 1, 50 (2007)
2. S. Cherry, Edholm's law of bandwidth. IEEE Spectr. **41**(7), 58–60 (2004)
3. C.E. Shannon, Communication in the presence of noise. Proc. IEEE **72**(9), 1192–1201 (1984)
4. D. Cabric, M.S.W. Chen, D.A. Sobel, Y. Jing, R.W. Brodersen, Future wireless systems: UWB, 60GHz, and cognitive radios. *IEEE Custom Integrated Circuits Conference*, Sept. 2005, pp. 793–796
5. R.C. Daniels, R.W. Heath, 60 GHz wireless communications: emerging requirements and design recommendations. IEEE Vehicular Technol. Mag. **2**(3), 41–50 (2007)
6. H. Lehpamer, Millimeter-Wave Radios in Backhaul Networks, Tech. Report, Communication Infrastructure Cooperation, 2008
7. C.H. Doan, S. Emami, D. Sobel, A.M. Niknejad, R.W. Brodersen, 60 GHz CMOS radio for Gb/s wireless LAN. *IEEE Radio Frequency Integrated Circuits Symposium*, June 2004, pp. 225–228
8. C.H. Doan, S. Emami, A.M. Niknejad, R.W. Brodersen, Design of CMOS for 60GHz applications. *IEEE International Solid-State Circuits Conference*, Feb. 2004, pp. 440–538
9. B. Floyd, U. Pfeiffer, S. Reynolds, A. Valdes-Garcia, C. Haymes, Y. Katayama, D. Nakano, T. Beukema, B. Gaudier, M. Soyuer, Silicon millimeter-wave radio circuits at 60-100 GHz. *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Jan. 2007, pp. 213–218
10. B.A. Floyd, S.K. Reynolds, U.R. Pfeiffer, T. Zwick, T. Beukema, B. Gaucher, SiGe bipolar transceiver circuits operating at 60 GHz. IEEE J. Solid-State Circuits **40**(1), 156–167 (2005)
11. B.A. Floyd, A 16-18.8-GHz sub-integer-N frequency synthesizer for 60-GHz transceivers. IEEE J. Solid-State Circuits **43**(5), 1076–1086 (2008)
12. T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi, I. Seto, A 60-GHz CMOS receiver front-end with frequency synthesizer. IEEE J. Solid-State Circuits **43**(4), 1030–1037 (2008)
13. A. Parsa, B. Razavi, A new transceiver architecture for the 60-GHz band. IEEE J. Solid-State Circuits **44**(3), 751–762 (2009)
14. S. Pinel, S. Sarkar, P. Sen, B. Perumana, D. Yeh, D. Dawn, J. Laskar, A 90 nm CMOS 60 GHz radio. *IEEE International Solid-State Circuits Conference*, Feb. 2008, pp. 130–601
15. S.K. Reynolds, B.A. Floyd, U.R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, M. Soyuer, A silicon 60-GHz receiver and transmitter chipset for broadband communications. IEEE J. Solid-State Circuits **41**(12), 2820–2831 (2006)

16. S. Sarkar, P. Sen, B. Perumana, D. Yeh, D. Dawn, S. Pinel, J. Laskar, 60 GHz single-chip 90nm CMOS radio with integrated signal processor. *IEEE International Microwave Symposium*, June 2008, pp. 1167–1170
17. M. Tanomura, Y. Hamada, S. Kishimoto, M. Ito, N. Orihashi, K. Maruhashi, H. Shimawaki, TX and RX Front-Ends for 60GHz Band in 90nm Standard Bulk CMOS. *IEEE International Solid-State Circuits Conference*, Feb. 2008, pp. 558–635
18. A. Tomkins, R.A. Aroca, T. Yamamoto, S.T. Nicolson, Y. Doi, S.P. Voinigescu, A zero-IF 60GHz transceiver in 65nm CMOS with >> 3.5Gb/s links. *IEEE Custom Integrated Circuits Conference*, Sept. 2008, pp. 471–474
19. IEEE 802.15 WPAN Millimeter Wave Alternative PHY Task Group 3c (TG3c), http://www.ieee802.org/15/pub/TG3c.html, March 2009
20. WirelessHD, Wireless HD Specification Version 1.0 Overview, Res. Lab. Electron, M.I.T., Cambridge, MA, Tech. Report, Oct. 2007
21. ECMA International, Standard ECMA-387, High Rate 60GHz PHY, MAC and HDMI PAL, *ECMA International*, Tech. Report, Dec. 2008
22. B. Razavi, A mm-wave CMOS heterodyne receiver with on-chip LO and divider. *IEEE International Solid-State Circuits Conference*, Lille, France, Feb. 2007, pp. 188–596
23. S.K. Reynolds, B.A. Floyd, U.R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, M. Soyuer, A silicon 60-GHz receiver and transmitter chipset for broadband communications. IEEE J. Solid-State Circuits **41**(12), 2820–2831 (2006)
24. K. Scheir, G. Vandersteen, Y. Rolain, P. Wambacq, A 57-to-66GHz quadrature PLL in 45nm digital CMOS. *IEEE International Solid-State Circuits Conference*, Feb. 2009, pp. 494-495,495a
25. W.L. Chan, J.R. Long, A 56-to-65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS. IEEE J. Solid-State Circuits **43**(12), 2739–2746 (2008)
26. C. Vaucher, Architectures for RF frequency synthesizers, Ph.D. dissertation, Eindhoven University of Technology, 2001
27. D. Banerjee, *PLL Performance, Simulation and Design*, 4th edn. (Dog Ear Publishing, LLC, Indianapolis, IN, 2006)
28. P. Sakian, E. van der Heijden, H.M. Cheema, R. Mahmoudi, A. van Roermund, A 57-63 GHz Quadrature VCO in CMOS 65 nm. *IEEE European Microwave Integrated Circuits Conference*, Sept. 2009
29. Cascade Microtech, Layout Rules for GHz-Probing, Tech. Report, Jan 2002
30. S.A. Wartenberg, Selected topics in RF coplanar probing. IEEE Trans. Microw. Theory Tech. **51**(4), 1413–1421 (2003)
31. D. Kasperkovitz, D. Grenier, Travelling-wave dividers: a new concept for frequency division. Microelectron. Reliab. **16**(2), 127–134 (1977)
32. H.M. Cheema, R. Mahmoudi, M.A.T. Sanduleanu, A. van Roermund, A Ka band, static, MCML frequency divider, in standard 90nm-CMOS LP for 60 GHz applications. *IEEE Radio Frequency Integrated Circuits Symposium*, Atlanta, GA, June 2007, pp. 541–544
33. H. Knapp, H.D. Wohlmuth, M. Wurzer, M. Rest, 25 GHz static frequency divider and 25 Gb/s multiplexer in 0.12 μm CMOS. *IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2002, pp. 302–468
34. Y. Mo, E. Skafidas, R. Evans, I. Mareels, 50 GHz static frequency divider in 130 nm CMOS. IET Electron. Lett. **44**(4), 285–286 (2008)
35. J.O. Plouchart, K. Jonghae, H. Recoules, N. Zamdmer, T. Yue, M. Sherony, A. Ray, L. Wagner, A power-efficient 33 GHz 2:1 static frequency divider in 0.12 μm SOI CMOS. *IEEE Radio Frequency Integrated Circuits Symposium*, June 2003, pp. 329–332
36. L. Tai-Cheng, L. Hua-Chin, H. Keng-Jan, H. Yen-Chuan, C. Guan-Jun, A 40-GHz distributed-load static frequency divider. *IEEE Asian Solid-State Circuits Conference*, Nov. 2005, pp. 205–208
37. G. von Buren, C. Kromer, F. Ellinger, A. Huber, M. Schmatz, H. Jackel, A combined dynamic and static frequency divider for a 40GHz PLL in 80nm CMOS. *IEEE International Solid-State Circuits Conference,* Feb. 2006, pp. 2462–247

38. H.D. Wohlmuth, D. Kehrer, W. Simburger, A high sensitivity static 2:1 frequency divider up to 19 GHz in 120 nm CMOS. *IEEE Radio Frequency Integrated Circuits Symposium*, June 2002, pp. 231–234
39. B. Kim, D.N. Helman, P.R. Gray, A 30-MHz hybrid analog/digital clock recovery circuit in 2-μm CMOS. IEEE J Solid-State Circuits **25**(6), 1385–1394 (1990)
40. M. Yamashina, H. Yamada, An MOS current mode logic (MCML) circuit for low-power sub-GHz processors. IEICE Trans Electron **E75-C**(10), 1181–1187 (1992)
41. Ali M. Niknejad, H. Hashemi, mm-Wave Silicon Technology: 60 GHz and Beyond (Springer, 2008)
42. L. Bangli, C. Dianyong, W. Bo, C. Dezhong, T. Kwasniewski, A 43-GHZ static frequency divider in 0.13 μm standard CMOS. *Canadian Conference on Electrical and Computer Engineering*, May 2008, pp. 111–114
43. C. Jung-Yu, L. Shen-Iuan, A 4-54GHz static frequency divider with back-gate coupling. *International Symposium on VLSI Design, Automation and Test*, April 2007, pp. 1–4
44. D.D. Kim, C. Choongyeun, K. Jonghae, J.O. Plouchart, Wideband mmWave CML static divider in 65nm SOI CMOS technology. *IEEE Custom Integrated Circuits Conference,* Sept. 2008, pp. 627–634
45. E. Laskin, M. Khanpour, R. Aroca, K.W. Tang, P. Garcia, S.P. Voinigescu, A 95GHz receiver with fundamental-frequency VCO and static frequency divider in 65nm digital CMOS. *IEEE International Solid-State Circuits Conference*, Feb. 2008, pp. 180–605
46. D. Lim, K. Jonghae, J.O. Plouchart, C. Choongyeun, K. Daeik, R. Trzcinski, D. Boning, Performance variability of a 90GHz static CML frequency divider in 6nm SOI CMOS. *IEEE International Solid-State Circuits Conference*, Feb. 2007, pp. 542–621
47. J.O. Plouchart, K. Jonghae, V. Karam, R. Trzcinski, J. Gross, Performance variations of a 66GHz static CML divider in 90nm CMOS. *IEEE International Solid-State Circuits Conference*, Feb 2006, pp. 2142–2151
48. X.P. Yu, M.A. Do, J.G. Ma, K.S. Yeo, R. Wu, G.Q. Yan, 1 V 10 GHz CMOS frequency divider with low power consumption. IET Electron. Lett. **40**(8), 467–469 (2004)
49. S. Pellerano, S. Levantino, C. Samori, A.L. Lacaita, A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic frequency divider. IEEE J. Solid-State Circuits **39**(2), 378–383 (2004)
50. J. Yuan, C. Svensson, Multigigahertz TSPC circuits in deep submicron CMOS. Phys. Scripta **T79**, 283–286 (1999)
51. B.A. Floyd, L. Shi, Y. Taur, I. Lagnado, K.O. Kenneth, SOI and bulk CMOS frequency dividers operating above 15 GHz. IET Electron. Lett. **37**(10), 617–618 (2001)
52. Y. Hongyan, M. Biyani, K.O. Kenneth, A high-speed CMOS dual-phase dynamic-pseudo NMOS ($(DP)^2$) latch and its application in a dual-modulus prescaler. IEEE J. Solid-State Circuits **34**(10), 1400–1404 (1999)
53. Jan M. Rabaey, A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits: A Design Perspective* (Prentice-Hall, Englewoods Cliffs, NJ, 2003)
54. E. Lopelli, J. van der Tang, A. van Roermund, A sub-mA FH frequency synthesizer technique. *IEEE Radio Frequency Integrated Circuits Symposium*, June 2006
55. R.L. Miller, Fractional-frequency generators utilizing regenerative modulation. Proc IRE **27** (7), 446–457 (1939)
56. J. Lee, B. Razavi, A 40-GHz frequency divider in 0.18-μm CMOS technology. IEEE J. Solid-State Circuits **39**(4), 594–601 (2004)
57. L. Tang-Nian, B. Shuen-Yin, Y.J.E. Chen, A 60-GHz 0.13 μm CMOS divide-by-three frequency divider. IEEE Trans. Microw. Theory Tech. **56**(11), 2409–2415 (2008)
58. U. Singh, M.M. Green, High-frequency CML clock dividers in 0.13 μm CMOS operating up to 38 GHz. IEEE J. Solid-State Circuits **40**(8), 1658–1661 (2005)
59. B. Razavi, A study of injection locking and pulling in oscillators. IEEE J. Solid-State Circuits **39**(9), 1415–1424 (2004)
60. W. Hui, Z. Lin, A 16-to-18GHz 0.18-m Epi-CMOS divide-by-3 injection-locked frequency divider. *IEEE International Solid-State Circuits Conference*, Feb. 2006, pp. 2482–2491

61. C. Wei-Zen, K. Chien-Liang, 18 GHz and 7 GHz superharmonic injection-locked dividers in 0.25μm CMOS technology. *IEEE European Solid-State Circuits Conference*, Sept. 2002, pp. 89–92
62. C. Jun-Chau, L. Liang-Hung, Analysis and design of wideband injection-locked ring oscillators with multiple-input injection. IEEE J. of Solid-State Circuits **42**(9), 1906–1915 (2007)
63. L. Liang-Hung, C. Jun-Chau, A wide-band CMOS injection-locked ring oscillator. IEEE Microw. Wireless Components Lett. **15**(10), 676–678 (2005)
64. T. Haitao, C. Shanfeng, A.I. Karsilayan, J.S. Martinez, An injection-locked frequency divider with multiple highly nonlinear injection stages and large division ratios. IEEE Trans. Circuits Syst. II: Express Briefs **54**(4), 313–317 (2007)
65. C. Shanfeng, T. Haitao, S. Jose, l.K. Aydn, A fully differential low-power divide-by-8 injection-locked frequency divider up to 18 GHz. *IEEE Journal of Solid-State Circuits* 42(3), 583–591 (2007)
66. W. Hui, A. Hajimiri, A 19 GHz 0.5 mW 0.35 μm CMOS frequency divider with shunt-peaking locking-range enhancement. *IEEE International Solid-State Circuits Conference*, Feb. 2001, pp. 412–413, 471
67. M. Tiebout, A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider. IEEE J. Solid-State Circuits **39**(7), 1170–1174 (2004)
68. S.L. Jang, C.C. Liu, J.F. Huang, A wide locking range injection locked frequency divider with quadrature outputs. IEICE Trans Electron **E91-C**(3), 373–377 (2008)
69. D. Yanping, K.O. Kenneth, A 21-GHz 8-modulus prescaler and a 20-GHz phase-locked loop fabricated in 130-nm CMOS. IEEE J. Solid-State Circuits **42**(6), 1240–1249 (2007)
70. P. Staric, E. Margan, *Wideband Amplifiers* (Springer, Dordrecht, The Netherlands, 2007)
71. C. Wei-Zen, C. Wen-Hui, H. Kuo-Ching, Three-dimensional fully symmetric inductors, transformer, and balun in CMOS technology. IEEE Trans. Circuits Systems I: Regular Papers **54**(7), 1413–1423 (2007)
72. W. Chia-Hsin, T. Chih-Chun, L. Shen-Iuan, Analysis of on-chip spiral inductors using the distributed capacitance model. IEEE J. Solid-State Circuits **38**(6), 1040–1044 (2003)
73. T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits* (Cambridge University Press, New York, 2003)
74. R. Adler, A study of locking phenomena in oscillators. Proc. IRE **34**(6), 351–357 (1946)
75. S. Verma, H.R. Rategh, T.H. Lee, A unified model for injection-locked frequency dividers. IEEE J. Solid-State Circuits **38**(6), 1015–1027 (2003)
76. H.R. Rategh, T.H. Lee, Superharmonic injection-locked frequency dividers. IEEE J. Solid-State Circuits **34**(6), 813–821 (1999)
77. B. Razavi, *Design of Integrated Circuits for Optical Communications* (McGraw-Hill Science, New York, 2002)
78. P. Andreani, A. Bonfanti, L. Romano, C. Samori, Analysis and design of a 1.8-GHz CMOS LC quadrature VCO. IEEE J. Solid-State Circuits **37**(12), 1737–1747 (2002)
79. X.P. Yu, H.M. Cheema, R. Mahmoudi, A. van Roermund, X.L. Yan, A 3 mW 54.6 GHz divide-by-3 injection locked frequency divider with resistive harmonic enhancement. IEEE Microw. Wireless Components Lett. **19**(9), 575–577 (2009)
80. J. Lin, M. Jian-Guo, S.Y. Kiat, A.D. Manh, 9.3-10.4-GHz-band cross-coupled complementary oscillator with low phase-noise performance. IEEE Trans. Microw. Theory Tech. **52**(4), 1273–1278 (2004)
81. J. Jin, X.P. Yu, J.J. Zhou, T.T. Yan, Gigahertz range injection locked frequency dividers with band-width enhancement and supply rejection. IET Electron. Lett. **44**(17), 999–1000 (2008)
82. V. Aparin, G. Brown, L. E. Larson, Linearization of CMOS LNA's via optimum gate biasing. *IEEE International Symposium on Circuits and Systems*, May 2004, pp. IV-748–IV-751
83. C. Hsien-Ku, C. Da-Chiang, J. Ying-Zong, L. Shey-Shi, A 30-GHz wideband low-power CMOS injection-locked frequency divider for 60-GHz wireless-LAN. IEEE Microw. Wireless Components Lett. **18**(2), 145–147 (2008)

84. H.K. Chen, C. Hsien-Jui, D.C. Chang, Y.Z. Juang, Y. Yu-Che, S.S. Lu, A mm-wave CMOS multimode frequency divider. *IEEE International Solid-State Circuits Conference*, Feb. 2009, pp. 280–281,281a
85. D.J. Cassan, J.R. Long, A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18μm CMOS. IEEE J. Solid-State Circuits **38**(3), 427–435 (2003)
86. C. Jun-Chau, L. Liang-Hung, 40GHz wide-locking-range regenerative frequency divider and low-phase-noise balanced VCO in 0.18μm CMOS. *IEEE International Solid-State Circuits Conference*, Feb. 2007, pp. 544–621
87. L. Shao-Hua, S.L. Jang, C. Yun-Hsueh, A low voltage divide-by-4 injection locked frequency divider with quadrature outputs. IEEE Microw. Wireless Components Lett. **17**(5), 373–375 (2007)
88. L. Tang-Nian, Y.J.E. Chen, A 0.8-mW 55-GHz dual-injection-locked CMOS frequency divider. IEEE Trans. Microw. Theory Tech. **56**(3), 620–625 (2008)
89. J. van der Tang, High-Frequency Oscillator Design for Integrated Transceivers, Ph.D. dissertation, Eindhoven University of Technology, 2002
90. A. Hajimiri, S. Limotyrakis, T.H. Lee, Jitter and phase noise in ring oscillators. IEEE J. Solid-State Circuits **34**(6), 790–804 (1999)
91. J.O. Plouchart, K. Jonghae, N. Zamdmer, M. Sherony, T. Yue, Y. Meeyoung, M. Talbi, A. Ray, L. Wagner, A 31 GHz CML ring VCO with 5.4 ps delay in a 0.12 μm SOI CMOS technology. *IEEE European Solid-State Circuits Conference*, Sept. 2003, pp. 357–360
92. W. Hui, A. Hajimiri, Silicon-based distributed voltage-controlled oscillators. IEEE J. Solid-State Circuits **36**(3), 493–502 (2001)
93. L. Lianming, P. Reynaert, M. Steyaert, A 90nm CMOS mm-wave VCO using an LC tank with inductive division. *IEEE European Solid-State Circuits Conference*, Sept. 2008, pp. 238–241
94. K.W. Tang, S. Leung, N. Tieu, P. Schvan, S.P. Voinigescu, Frequency scaling and topology comparison of millimeter-wave CMOS VCOs. *IEEE Compound Seminconductor Integrated Circuit Symposium*, Nov. 2006, pp. 55–58
95. B. Heydari, M. Bohsali, E. Adabi, A.M. Niknejad, Millimeter-wave devices and circuit blocks up to 104 GHz in 90 nm CMOS. IEEE J. Solid-State Circuits **42**(12), 2893–2903 (2007)
96. L.M. Franca-Neto, R.E. Bishop, B.A. Bloechel, 64 GHz and 100 GHz VCOs in 90 nm CMOS using optimum pumping method. *IEEE International Solid-State Circuits Conference*, Feb. 2004, pp. 444–538
97. C. Changhua, K.O. Kenneth, Millimeter-wave voltage-controlled oscillators in 0.13-μm CMOS technology. IEEE J. Solid-State Circuits **41**(6), 1297–1304 (2006)
98. A.P. van der Wel, S.L.J. Gierkink, R.C. Frye, V. Boccuzzi, B. Nauta, A robust 43-GHz VCO in CMOS for OC-768 SONET applications. IEEE J. Solid-State Circuits **39**(7), 1159–1163 (2004)
99. D.B. Leeson, A simple model of feedback oscillator noise spectrum. Proc. IEEE **54**(2), 329–330 (1966)
100. J.J. Rael, A.A. Abidi, Physical processes of phase noise in differential LC oscillators. *IEEE Custom Integrated Circuits Symposium*, May 2000, pp. 569–572
101. A. Hajimiri, T.H. Lee, A general theory of phase noise in electrical oscillators. IEEE J. Solid-State Circuits **33**(2), 179–194 (1998)
102. J. Craninckx, M. Steyaert, Low-noise voltage-controlled oscillators using enhanced LC-tanks. IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process. **42**(12), 794–804 (1995)
103. B. Razavi, A study of phase noise in CMOS oscillators. IEEE J. Solid-State Circuits **31**(3), 331–343 (1996)
104. E. Hegazi, H. Sjoland, A.A. Abidi, A filtering technique to lower LC oscillator phase noise. IEEE J. Solid-State Circuits **36**(12), 1921–1930 (2001)
105. R. Aparicio, A. Hajimiri, A CMOS differential noise-shifting Colpitts VCO. *IEEE International Solid-State Circuits Conference*, Feb. 2002, pp. 288-289

106. P. Andreani, S. Mattisson, On the use of MOS varactors in RF VCOs. IEEE J. Solid-State Circuits **35**(6), 905–910 (2000)
107. H. Ainspan, J.O. Plouchart, A comparison of MOS varactors in fully-integrated CMOS LC VCO's at 5 and 7 GHz. *IEEE European Solid-State Circuits Conference*, Sept. 2000, pp. 447–450
108. N. Fong, G. Tarr, N. Zamdmer, J.O. Plouchart, C. Plett, Accumulation MOS varactors for 4 to 40 GHz VCOs in SOI CMOS. *IEEE International SOI Conference*, Oct. 2002, pp. 158–160
109. T. Soorapanth, C. P. Yue, D. K. Shaeffer, T. I. Lee, S. S. Wong, Analysis and optimization of accumulation-mode varactor for RF ICs. *IEEE Symposium on VLSI Circuits*, June 1998, pp. 32–33
110. K. Jonghae, J.O. Plouchart, N. Zamdmer, R. Trzcinski, W. Kun, B.J. Gross, K. Moon, A 44GHz differentially tuned VCO with 4GHz tuning range in 0.12 μm SOI CMOS. *IEEE International Solid-State Circuits Conference*, Feb. 2005, pp. 416–607
111. N. Fong, J.O. Plouchart, N. Zamdmer, L. Duixian, L. Wagner, C. Plett, G. Tarr, A 1 V 3.8-5.7 GHz differentially-tuned VCO in SOI CMOS. *IEEE Radio Frequency Integrated Circuits Symposium*, June 2002, pp. 75–78
112. M. Tiebout, Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS. *IEEE Journal of Solid-State Circuits* 36(7), 1018–1024 (2001)
113. J.P. Carr, B.M. Frank, A 38 GHz accumulation MOS differentially tuned VCO design in 0.18-μm CMOS. *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Jan. 2006
114. F. Neric, K. Jonghae, J.O. Plouchart, N. Zamdmer, L. Duixian, L. Wagner, C. Plett, G. Tarr, A low-voltage 40-GHz complementary VCO with 15% frequency tuning range in SOI CMOS technology. *IEEE Journal of Solid-State Circuits*, 39(5), 841–846 (2004)
115. L. Tang-Nian, B. Shuen-Yin, E.C. Yi-Jan, C. Hsin-Shu, H. Deukhyoun, A 1-V CMOS VCO for 60-GHz applications. *IEEE Asia-Pacific Microwave Conference,* Dec. 2005.
116. D.D. Kim, K. Jonghae, J.O. Plouchart, C. Choongyeun, L. Weipeng, L. Daihyun, R. Trzcinski, M. Kumar, C. Norris, D. Ahlgren, A 70GHz manufacturable complementary LC-VCO with 6.14GHz tuning range in 65nm SOI CMOS. *IEEE International Solid-State Circuits Conference*, Feb. 2007, pp. 540–620
117. F. Ellinger, T. Morf, G. Buren, C. Kromer, G. Sialm, L. Rodoni, M. Schmatz, H. Jackel, 60 GHz VCO with wideband tuning range fabricated on VLSI SOI CMOS technology. *IEEE International Microwave Symposium*, June 2004, pp. 1329–1332
118. J. Borremans, M. Dehan, K. Scheir, M. Kuijk, P. Wambacq, VCO design for 60 GHz applications using differential shielded inductors in 0.13 μm CMOS. *IEEE Radio Frequency Integrated Circuits Symposium*, June 2008, pp. 135–138
119. K. Kwok, H.C. Luong, Ultra-low-Voltage high-performance CMOS VCOs using transformer feedback. IEEE J. Solid-State Circuits **40**(3), 652–660 (2005)
120. A.W.L. Ng, H.C. Luong, A 1-V 17-GHz 5-mW CMOS quadrature VCO based on transformer coupling. IEEE J. Solid-State Circuits **42**(9), 1933–1941 (2007)
121. L. Zhenbiao, K.O. Kenneth, A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator. IEEE J. Solid-State Circuits **40**(6), 1296–1302 (2005)
122. N.H.W. Fong, J.O. Plouchart, N. Zamdmer, L. Duixian, L.F. Wagner, C. Plett, N.G. Tarr, Design of wide-band CMOS VCO for multiband wireless LAN applications. IEEE J. Solid-State Circuits **38**(8), 1333–1342 (2003)
123. B. Catli, M.M. Hella, A 0.5-V 3.6/5.2 GHz CMOS multi-band LC VCO for ultra low-voltage wireless applications. *IEEE International Symposium on Circuits and Systems*, May 2008, pp. 996–999
124. A. Goel, H. Hashemi, Concurrent dual-frequency oscillators and phase-locked loops. IEEE Trans. Microw. Theory Tech. **56**(8), 1846–1860 (2008)
125. N.T. Tchamov, S.S. Broussev, I.S. Uzunov, K.K. Rantala, Dual-band LC VCO architecture with a fourth-order resonator. IEEE Trans. Circuits Syst. II: Express Briefs **54**(3), 277–281 (2007)

126. B. Catli, M.M. Hella, A dual band, wide tuning range CMOS voltage controlled oscillator for multi-band radio. *IEEE Radio Frequency Integrated Circuits Symposium*, June 2007, pp. 595–598
127. T. Sai-Wang, Y. Hsing-Ting, K. Yanghyo, E. Socher, M.C.F. Chang, T. Itoh, A dual band mm-wave CMOS oscillator with left-handed resonator. *IEEE Radio Frequency Integrated Circuits Symposium*, June 2009, pp. 477–480
128. R. Sujiang, H.C. Luong, A 1V 4GHz-and-10GHz transformer-based dual-band quadrature VCO in 0.18-μm CMOS. *IEEE Custom Integrated Circuits Conference*, Sept. 2007, pp. 817–820
129. A. Mazzanti, P. Uggetti, R. Battagia, F. Svelto, Analysis and design of a dual band reconfigurable VCO. *IEEE International Conference on Electronics, Circuits and Systems*, Dec. 2004, pp. 37–40
130. L.K.L. Lincoln, W.C.C. Kay, C.L. Howard, A 1V dual-band VCO using an integrated variable inductor. *IEEE Asian Solid-State Circuits Conference*, Nov. 2005, pp. 273–276
131. H.D. Wohlmuth, D. Kehrer, R. Thuringer, W. Simburger, A 17 GHz dual-modulus prescaler in 120 nm CMOS. *IEEE Radio Frequency Integrated Circuits Symposium*, June 2003, pp. 479–482
132. H.D. Wohlmuth, D. Kehrer, A 24 GHz dual-modulus prescaler in 90 nm CMOS. *IEEE International Symposium on Circuits and Systems*, May 2005, pp. 3227–3230
133. W. Hu, L. Chunglen, X. Wang, Fast frequency acquisition phase-frequency detector with zero blind zone in PLL. IET Electron. Lett. **43**(19), 1018–1020 (2007)
134. M. Mansuri, D. Liu, C.K.K. Yang, Fast frequency acquisition phase-frequency detectors for Gsamples/s phase-locked loops. IEEE J. Solid-State Circuits **37**(10), 1331–1334 (2002)
135. G.B. Lee, P.K. Chan, L. Siek, A CMOS phase frequency detector for charge pump phase-locked loop. *IEEE Midwest Symposium on Circuits and Systems*, 1999, pp. 601–604
136. H.O. Johansson, A simple precharged CMOS phase frequency detector. IEEE J. Solid-State Circuits **33**(2), 295–299 (1998)
137. H. Kondoh, H. Notani, T. Yoshimura, H. Shibata, Y. Matsuda, A 1.5-V 250-MHz to 3.0-V 622-MHz operation CMOS phase-locked loop with precharge type phase-frequency detector. IEICE Trans Electron **E78-C**(4), 381–388 (1995)
138. D. Mijuskovic, M. Bayer, T. Chomicz, N. Garg, F. James, P. McEntarfer, J. Porter, Cell-based fully integrated CMOS frequency synthesizers. IEEE J. Solid-State Circuits **29**(3), 271–279 (1994)
139. C. Changhua, D. Yanping, K.O. Kenneth, A 50-GHz phase-locked loop in 0.13-μm CMOS. IEEE J. Solid-State Circuits **42**(8), 1649–1656 (2007)